CATRENE: GIVER and TAKER for 3D Innovation

SEMI's European 3D TSV Summit
January 22nd 2014
Grenoble

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SPTS Technologies

- SPTS Technologies designs, manufactures, sells, and supports etch, PVD, CVD and thermal capital equipment, providing advanced wafer processing technologies for the microelectronics industry.
- Formed in 2009, SPTS brings together over 40 years wafer processing experience from companies including Watkins-Johnson, Trikon Technologies, STS, Aviza Technology and AMMS.
- The solutions offered by SPTS include market-leading silicon etch, dielectric etch, dry-release etch, PVD, PECVD, APCVD and large batch vertical furnaces
- SPTS Technologies sas (France) is a subsidiary of SPTS technologies dedicated for sales, support & service, R&D.

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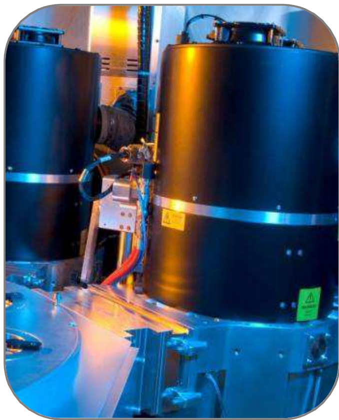
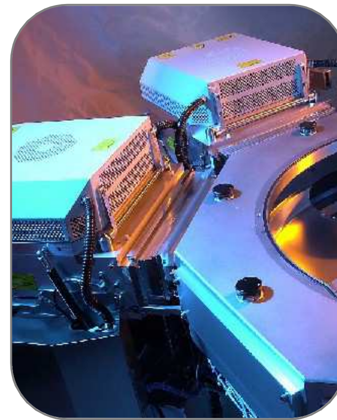
SPTS Technologies

SPTS

- Broad supplier of wafer processing solutions
  - For MEMS, compound semi, power and packaging markets
- Formed in Oct-09 via merger of former STS and Aviza
  - MBO in Jun-11
- Manufacturing sites in UK and US
  - Global presence with 35 worldwide locations


Etch

PVD


CVD

Thermal

Release Etch

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SPTS - *Global Presence*

Release Etch Manufacturing

Single Wafer Manufacturing

Thermal Products Manufacturing

Manufacturing Sites

Sales Offices

Service Centers

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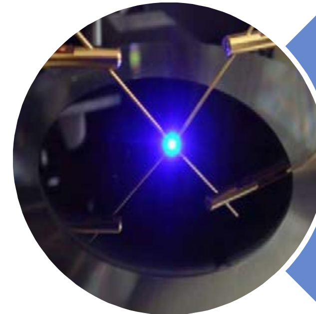
SPTS Equipment is Used for Making...

MEMS

- Micro Electro Mechanical Systems in inkjet heads, smart-phones, games consoles, and tablets

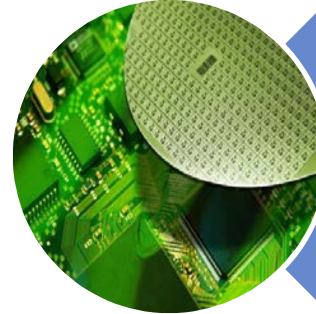


LEDs

- LED-backlit TVs, general indication, and automotive / industrial / domestic lighting

Power Devices

- Control / reduce / generate power used in electronic and power systems

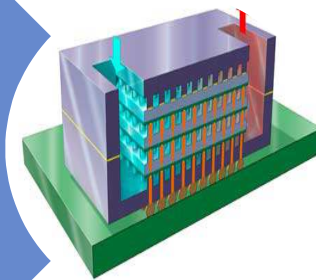


Semiconductor Devices

- Mainstream Si-based devices, including front-end CMOS/Logic/DRAM processing

Advanced Packaging

- Packaging semiconductor devices to reduce size and increase performance



High Speed Electronics

- Electronic devices using III-V materials to increase the speed /performance in devices

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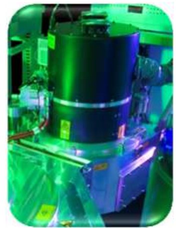
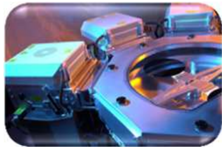
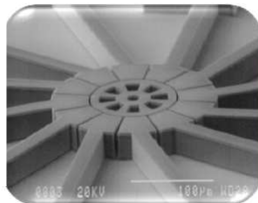
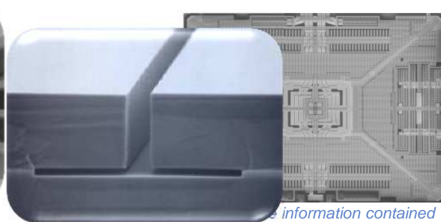
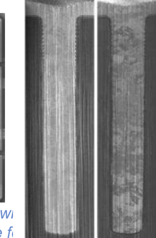
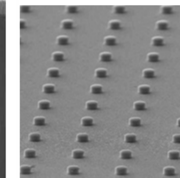
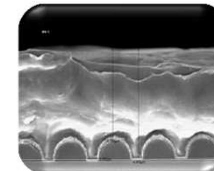
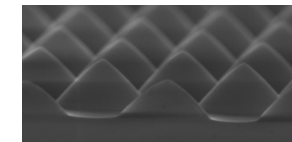
SPTS Solutions

Products	MEMS	Adv Packaging	Power	Compound
Etch Omega	Deep Si Deep oxide	TSV Oxide liner Via reveal	Active trenches Deeper trenches SiC, GaN	Backside Vias Dielectrics SiC, GaN Sapphire
CVD Delta	Low stress SiN Low temp for TSV High RI etch mask	Low temp TSV liners Via reveal SiN, SiO Tuned stack stress		MIMCAP SiN Ammonia free SiN Dense SiN passivation
PVD Sigma	Piezo AlN Bolometer Resistors Low Stress Al Motion Sensor Electrodes	UBM/RDL TSV Cu Barrier/Seed Si & Mold Wafers	Thick Al, Cu W-Plug Liner/Barrier Thin Wafer BSM SiC, GaN	Backside Via TFR SAW SiOx BAW AlN
Release division Primaxx–vapor HF Xactix–vapor XeF2	Dry oxide release/ Dry silicon release			
Thermal AVP/RVP	Low stress SiN Thick poly-Si Low temp SiGe	FO-WLP anneals Tox/LPCVD liners Cu anneal	Drive-in anneal Tox/LPCVD liners Poly-Si trench fill	Low temp anneal

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Single Wafer Products Division

- Location
  - Newport, South Wales, UK
- 104,200 sq ft
- 22 Universal Test Cells
- 15 Universal Assembly Cells
- 5S-Controlled Class 1000 cleanroom environment
- Flexible, multi-skilled workforce
- Lean culture with value-stream mapping
- Practice Design-for-manufacturing (DFM)

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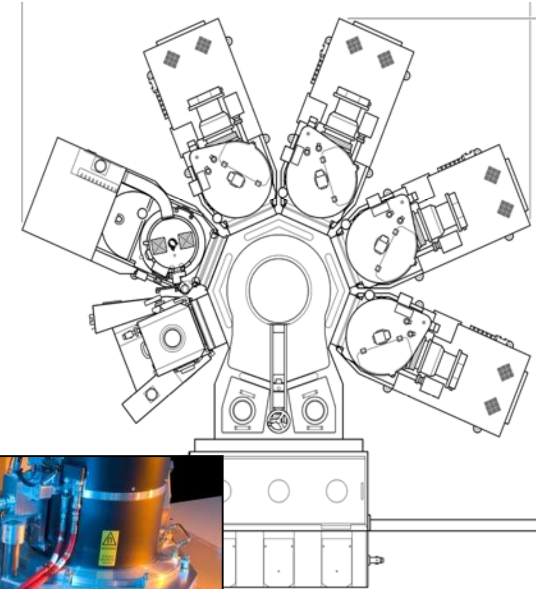
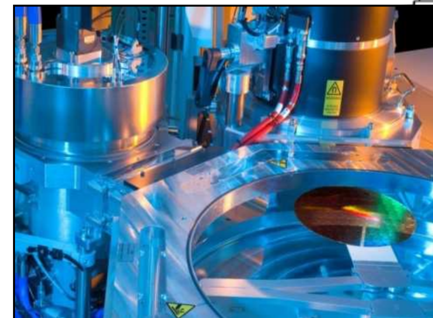
SPTS Product Strategy in 3D

- Started with WLCSP in 2005
  - 1st generation TSV, for CMOS image sensors
  - Now used for fingerprint sensors
  - Still highest volume TSV device
- Offering for 2.5 and 3D stacking
  - Etch: Via etch and via reveal
  - DCVD: Via isolation & via reveal
  - PVD: TSV metals & bump/RDL
- Product strategy
  - High productivity, low CoO.
  - Film stability at low temp
- Running on…
  - Single technology systems
  - Or multi-tech on one platform





Versalis *fx*P
PVD, etch and CVD on one platform
Ideal for R&D, pilot
Saves capex $$ & floorspace

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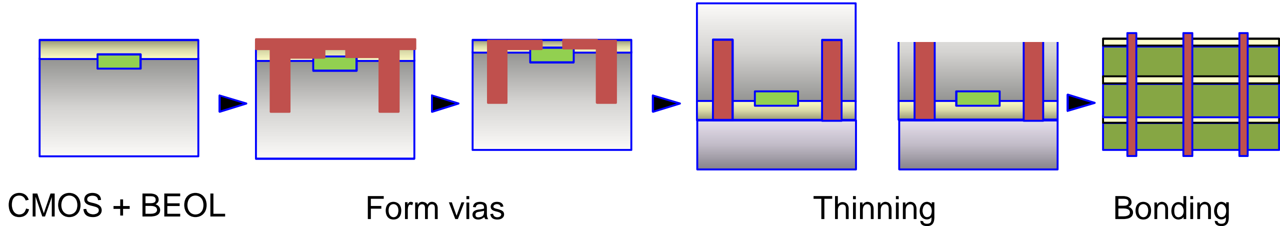
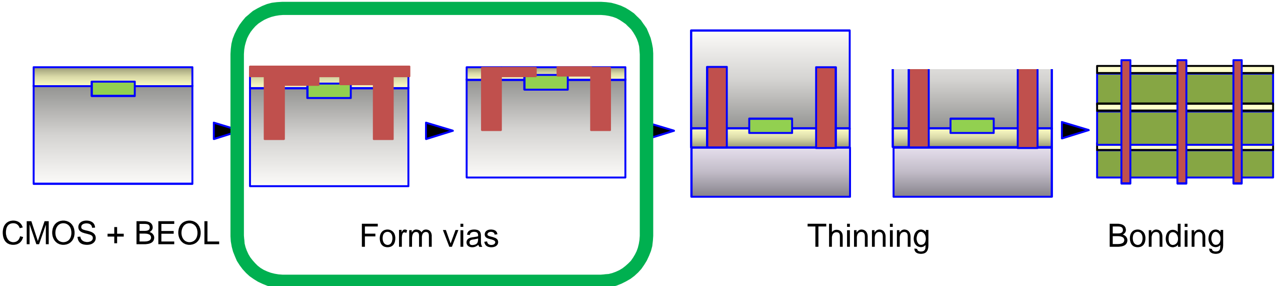
Projects contribution

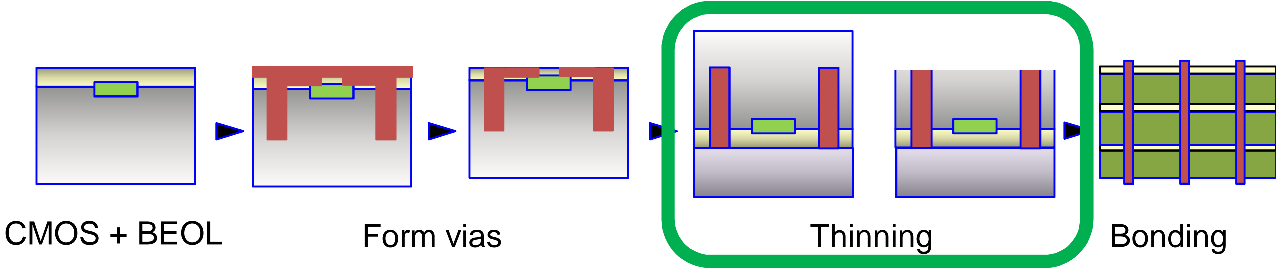
- 3D process flow



- SPTS contribution
  - Vias : Etch, Deposition (insulation, Metal : barrier, seed)



  - Vias reveal



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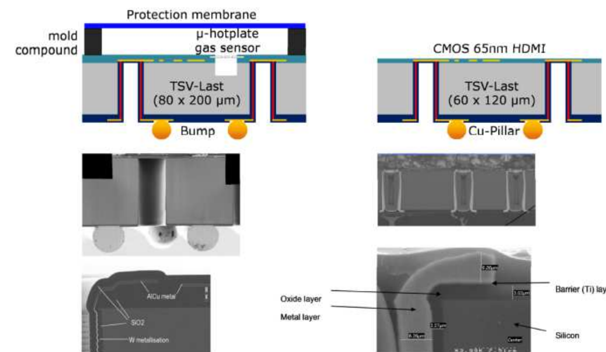
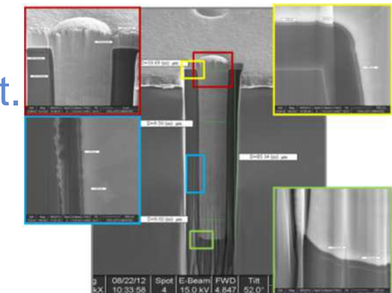
Projects contribution

SPTS

- CATRENE Projects
  - COCOA
    - 3D integration technology platform covering all processes required from vertical interconnects and robust bonding to innovative packaging to address new 3D products (6:1 & 20:1 A.R Vias).
    - Realization of product demonstrators for multimedia and wireless applications and sensor integration applications.



  - Master 3D
    - 3D ICs with Through Silicon Vias (TSV) and Wafer Level Packaging (WLP).
    - **Tool enhancements to support high yield, mass production**
    - Functional and Final Test concepts
    - Characterization and in-line Metrology methods development.



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Projects Collaboration & benefits

SPTS

- Direct discussion between all partners from R&D lab to end users
- Collaboration with labs :
  - Validate concept & feasability of advanced recipes & hardware
- Collaboration with end users
  - Define precisely process perf. specification
  - Aim to demonstrate the robustness and stability of processes & tools
- Collaboration with other equipement Vendors
  - Understand complete process flow specifications & limitations

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Why to chose CATRENE?

- Catrene offers to grant one part of the strategic R&D and product development
- Catrene offers an easy & free way of communication with all 3D actors from equipement vendors to IDMs
- Catrene offers us the possibility to demonstrate our tools & process capabilities for new technologies for IDMs on full demonstrators

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