FROM RESEARCH TO INDUSTRY

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leti & list

New possibilities offered by 3D

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Key message: 3D is impacting semiconductor markets

- IC markets are dominated by computing i.e Logic, Memory and I/O;
- The key challenges for future high-end computing chips are Yield/Cost, power, data transfer and I/O, Heterogeneous Integration
- 3D is Happening
  - To improve yield cost and power
  - to shorten distances and increase bandwidth in a single chip, … But off-chip I/O will be the bottleneck. Si-Photonics will be soon required for chip to chip on board and later on Interposer (2.5D)
  - To enable Heterogeneous Integration
- Implications on semiconductor will be disruptive

Agenda

- The semiconductor Market
- 3 Top Trends in Semiconductors
  - 3D to master Cost , Yield and Power
  - 3D to master on chip and off chip Interconnect
  - 3D to enable Heterogeneous Integration
- Implications on Semiconductor

IC Market

From 270 B$ (2012) to 460B$ (2019) <IBS 2012>

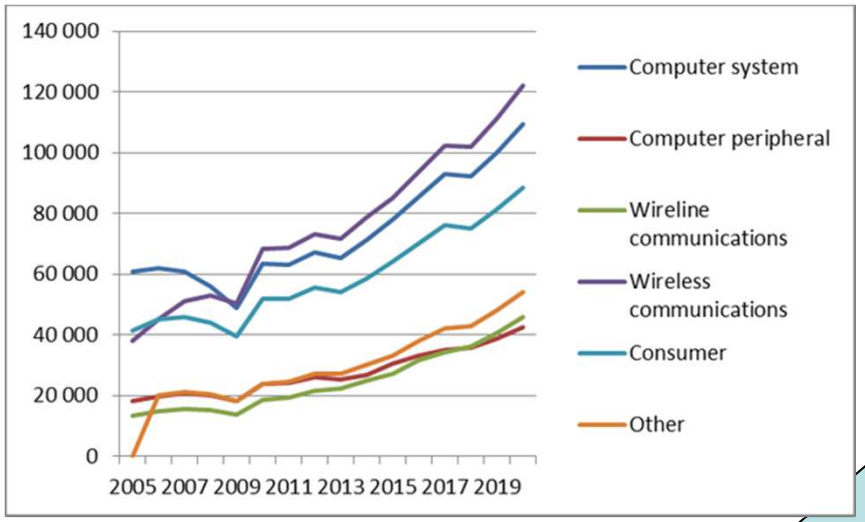
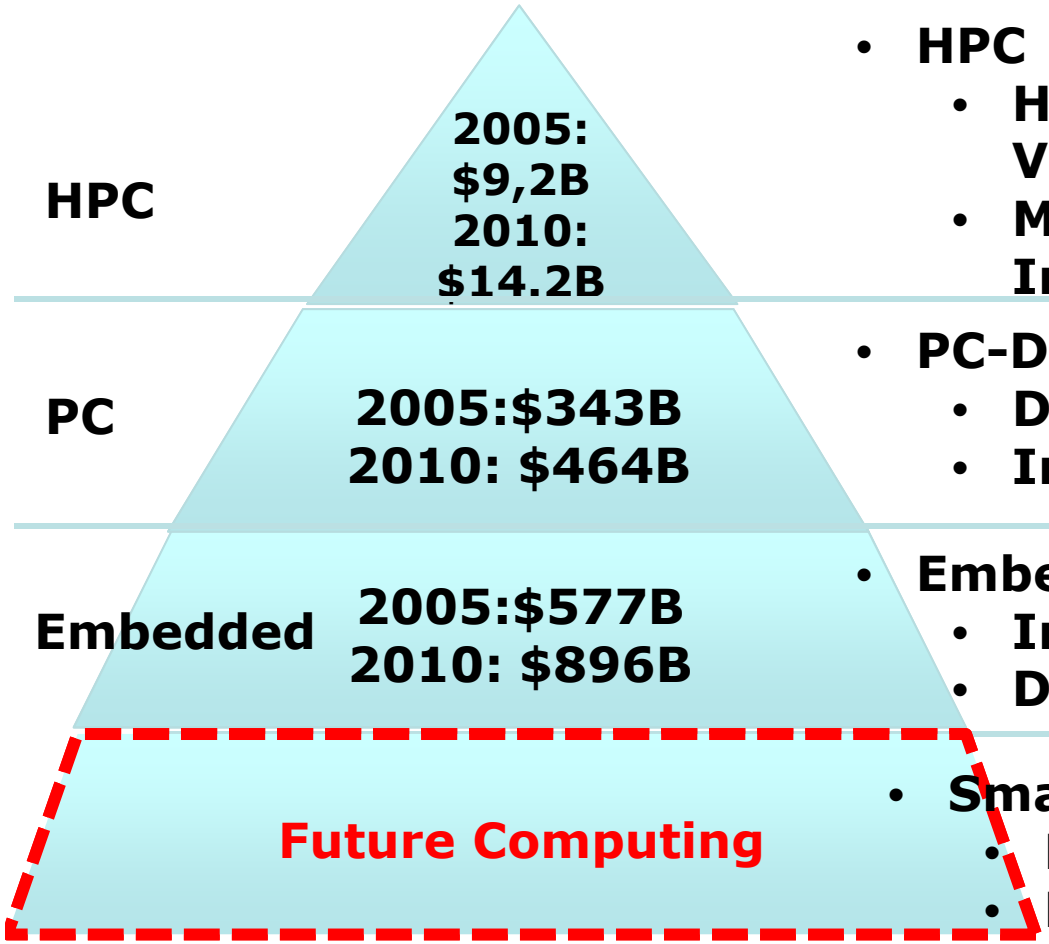


Figure 2. Application-Driven Family Tree

Computing Impacts larger Sectors



- **HPC**
  - **High End HPC Systems 25% Volume HPC Market, 75%**
  - **Main Driver of Semiconductor Industry in 80's**
- **PC-Desktop Market**
  - **Driver of Semiconductor in 90's**
  - **Introduced use of COTS**
- **Embedded Market**
  - **Introduced use of IP,**
  - **Driver of semiconductor in 2000's**
- **Smart systems; IoT**
  - **New integration concepts**
  - **Driving semiconductor in 2010's**

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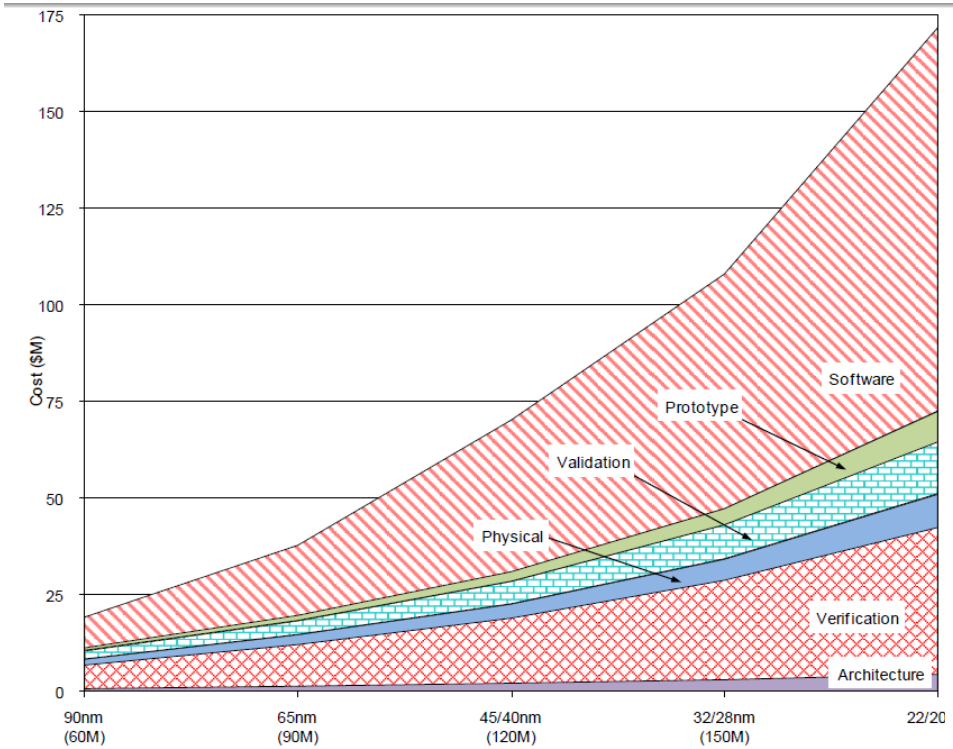
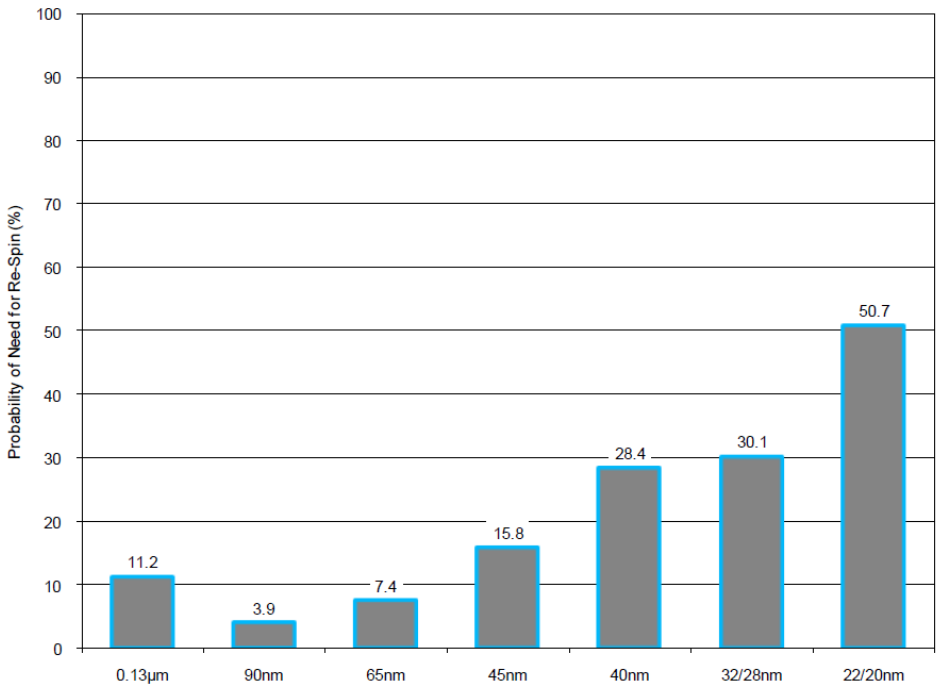
The cost and yield challenges



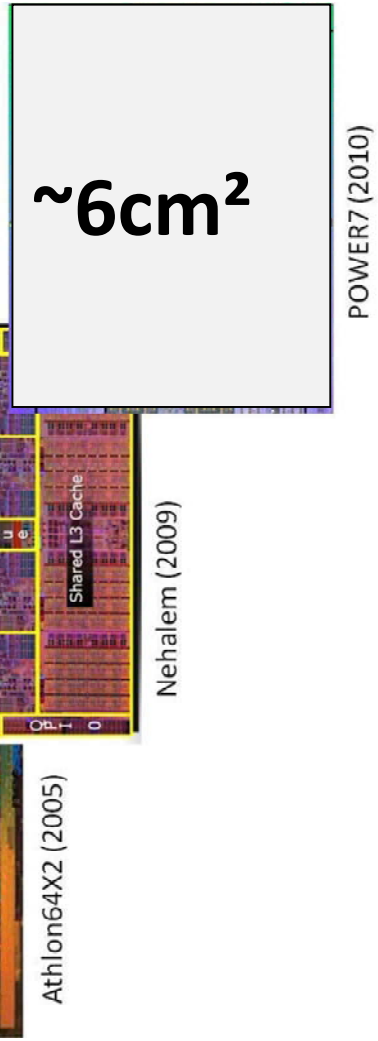


[Source IBS]

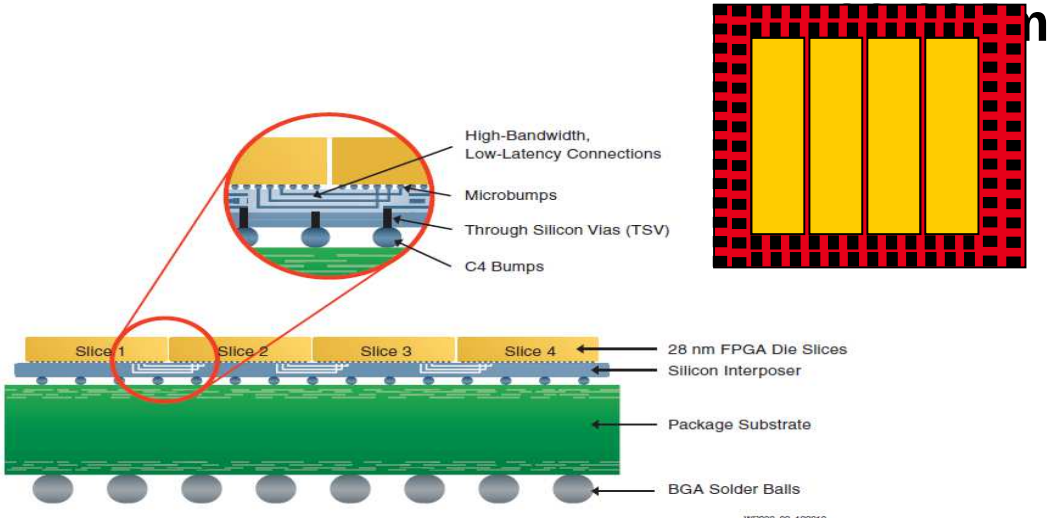
- **Productivity crisis**
  - **Design Cost is rocketing, 170M$ 22 nm**
- **Time to Market Crisis for**
  - **Design Respin rate reaching 50% for 22nm**

Implications

- The reticule Wall
  - Maximum Integration on chip (6cm², 100+W)
  - Main semiconductor manufacturing drivers
  - High performances IC (CPU, GPU, FPGA)



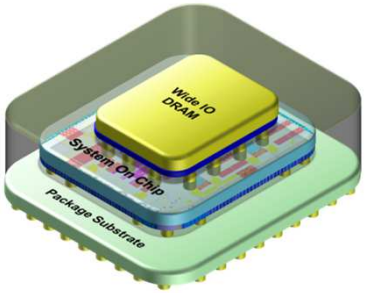
- The wall of Yield, cost, packaging …



3D-IC Xilinx 28 nm

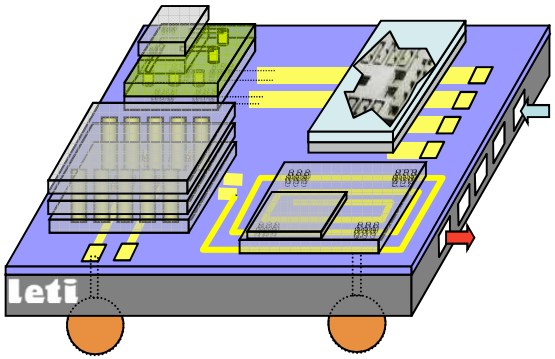
3D integration is happening

3D SoC



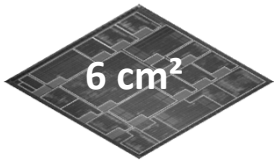
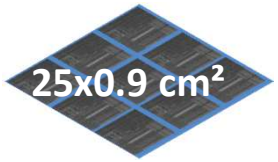
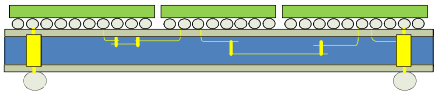
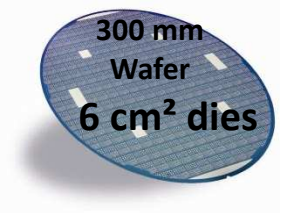
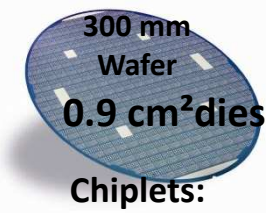
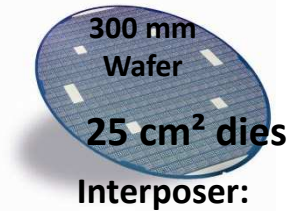
- 3D-stacked dies
- Memory-on-processor:
  - 3D memory hierarchy
- Processor-on-processor:
  - Many-core cluster
- High bandwidth
- Fine grain architecture partitioning
- High density for vertical interconnects
- Face-to-back

Silicon board



- Dies stacked on a silicon interposer
- Heterogeneous integration:
  - Digital, analog, memory, input/output, power management
- Medium bandwidth
- System partitioning
- High density for horizontal interconnects
- Face-to-face
- Large size silicon interposer

Silicon Board concept to reduce cost and … Power

	Traditional technology	Silicon Board concept
	Large IC with maximum integration on chip	Small dies stacked on a large interposer
	 1 die  3Ghz	 200Mhz  25 chiplets+ 1 interposer
Die cost	5000 $ wafer cost 89 dies of 6 cm² 20% yield → 281 $ die cost  → 281 $ die cost	Same cost 6 cm² versus 25 cm²  Chiplets: 5000 $ wafer cost 714 dies of 0.9 cm² 80% yield → 8.75 $ die cost  Interposer: 500 $ wafer cost 14 dies of 25 cm² 98% yield → 36.44 $ die cost → 255 $ total die cost
IC cost*	95% final test yield → 296 $ IC cost	90% final test yield → 284 $ 3D-IC cost
	2 GFLOPS/W	More than 50x energy efficiency — 100 GFLOPS/W

*: test and package costs are not included but considered equal for both technologies in this exercise

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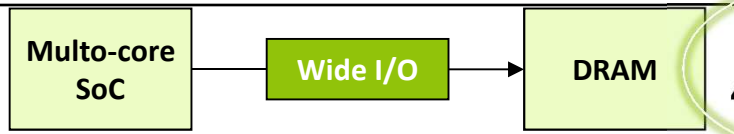
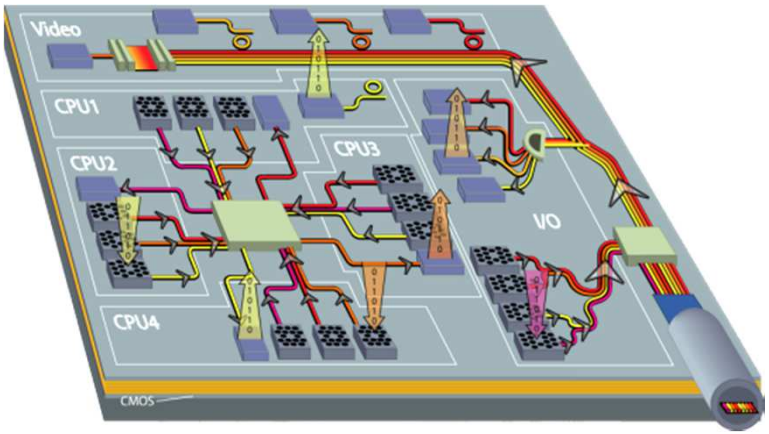
The Transfer Density Challenge

- Memory-interconnect density is becoming the bottleneck

Memory link, peak bandwidth and power consumption efficiency	Cost for 1TBps memory bandwidth	
	Number of data IO pins	Interface power consumption
 8.532 GBps 30 mW/Gbps 1066 MHz I/O bus clock, 32 bits, 1.5 V, Double Data Rate	3 800 Offchip	240 W
 6.4 GBps 20 mW/Gbps 800 MHz I/O bus clock, 32 bits, 1.2 V, Double Data Rate	5000 Off-chip	160 W
 12.8 GBps 4 mW/Gbps 200 MHz I/O bus clock, 512 bits, 1.2 V, Single Data Rate	41 000 Off-chip	32 W
 >TBps 1 mW/Gbps Assume 200 MHz 50K pins connected to SERDES to Photonics	50 000 on chip + 40 Wavelengths (or 40 Wave guides) at 25Gbs	8 W + MUX-DEMUX?

Why Si Photonics?

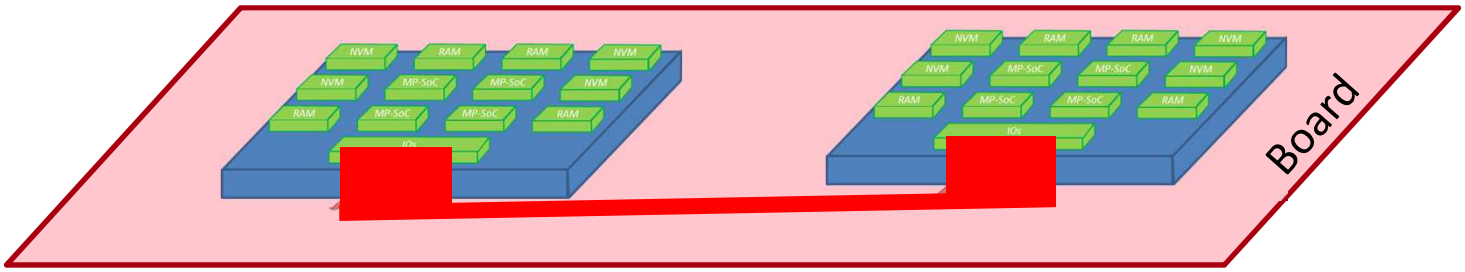
- **Si Photonics vs Electrical transfer**
  - **Less energy than electrical-only (distance dependant)**
    - 10Mb/s , 1km: ADSL
    - 10Gb/s , 1m: Inter Rack
    - 100Gb/s , 10cm: Chip to Chip on (Silicon) Board
    - 1Tb/s , 1cm: Silicon Board
  - **Higher I/O bandwidth density**
- **3D accelerates Photonics Roadmaps**



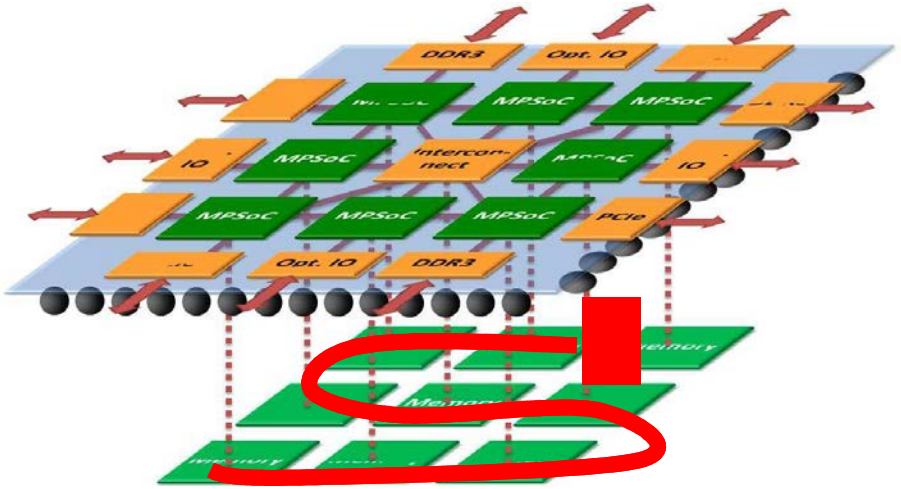
Data transfer Bottleneck for 1 TFLOP SOC

- **1 TFLOPs SoC / 10W doable in short tem (2014)**
- **Off-chip I/O (10Tb/s) 1 TFLOPs => 1 TB/s**
  - Electrical solution:
    - 5pJ/b @ 10Gb/s = 50 mW/b
    - 1000 differential pin pairs 40W
- **On Chip I/O**
  - Bisection wires: 50Tb/s
- **Hitting the I/O density limit**
  - Silicon Photonics Solution is efficient at 1Tb/s/cm !!!!!!

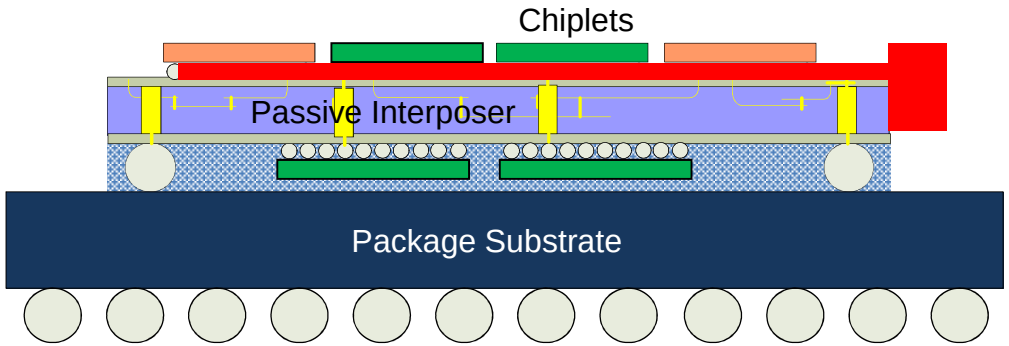
<10 cm Chip to Chip Optical Link required for SoC



More Integration in the Roadmap



- **10 TFLOP SoC doable using Double sided Interposer**
- **Off-chip I/O 100Tb/s**
- **On Chip I/O**
  - Bisection wires: 50Tb/s



On Interposer Optical Link required for 10 TFLOP SoC

May require new Partitioning-architecture of the Photonic Link

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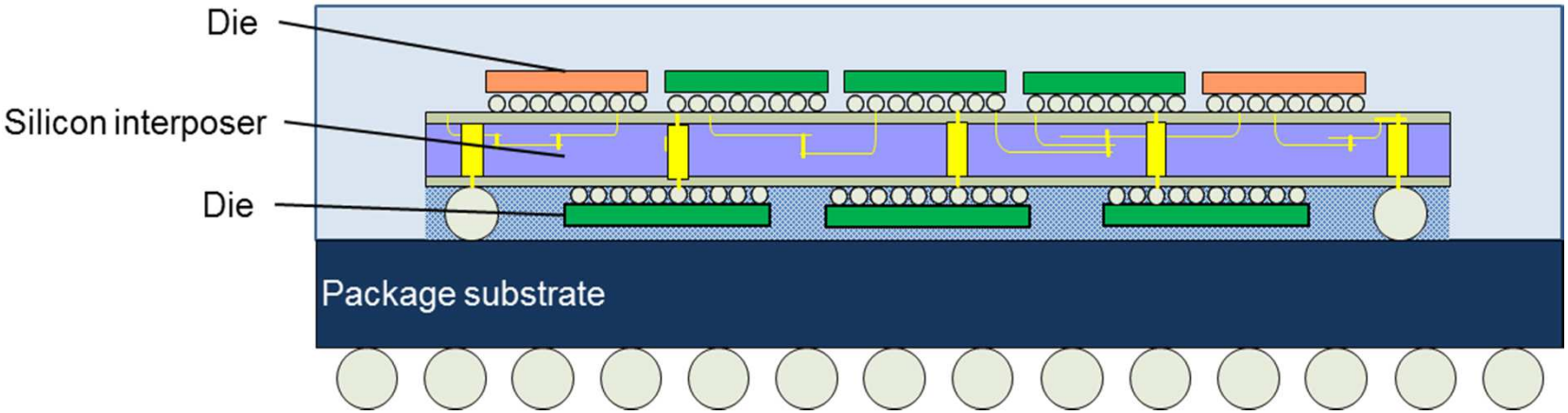
Silicon Board for Heterogeneous Integration

Backbone for heterogeneous integration of small dies, passives and photonics → miniaturization



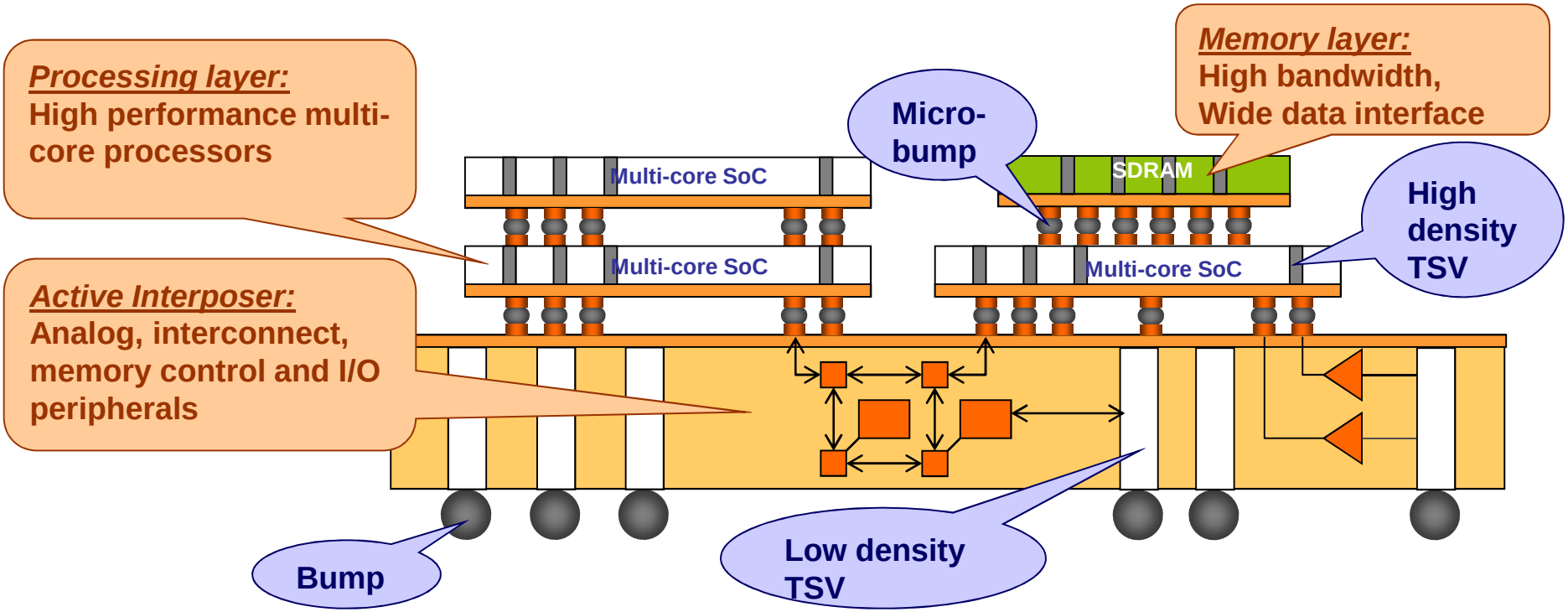
Interconnect with very low capacitive and inductive load

→ energy efficiency

Silicon Board for Heterogeneous Integration

- Heterogeneous integration rationale:
  - Digital logic shrinks significantly with process technology
  - Small dies shorten new process introduction and improve overall yield
  - Analog design and IOs doesn't shrink a lot with process technology
  - Short interconnect improves signal and power integrity

→ The SoC is partitioned into several dies, each of one being processed with the most relevant technology node in terms of performance and cost



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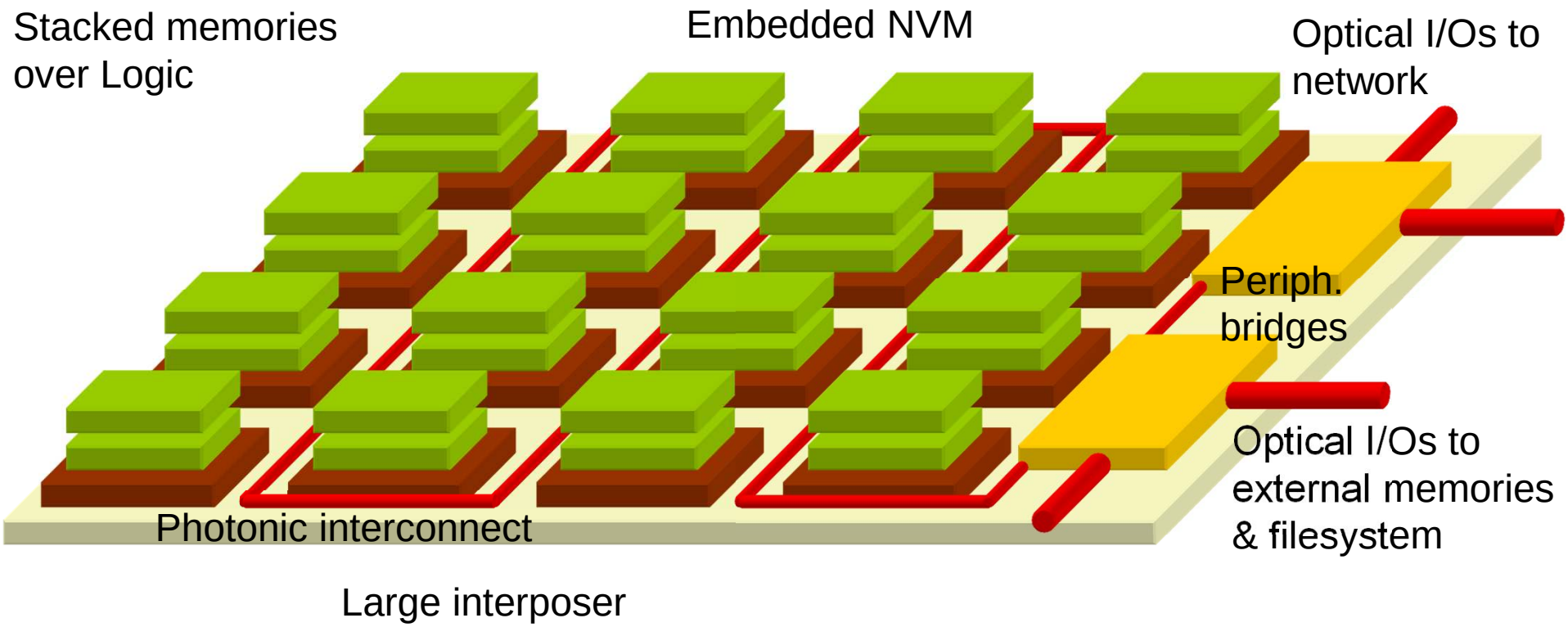
Implication of 3D on IC design

- Contents of a single package:



Roadmap for Silicon Demonstrators

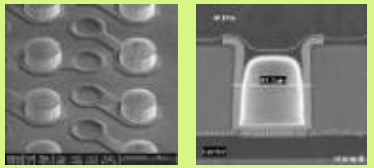
Technology add-on

Core 3D Technology (200 & 300 mm)

Mechanical Stress management modules *(stress buffer, compliant int.)*

TSV *Cu Damascene line*

Bonding Thinning RDL Bumps TSV last



Stacking *Interconnects, underfill, P&P*

Thermal management modules

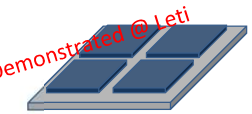
Bio Techno Modules *Biocomp,…*

Specific packaging solutions *Dicing, direct-on-board, bio-compatibility*

Modules for RF *(integrated antenna)*

Silicon on Flex Modules

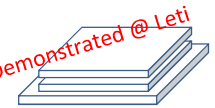
Today 2012-2013



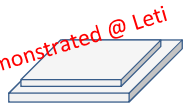
Si interposer

TSV Ø10µm, 50µm pitch

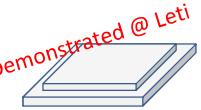
Tomorrow 2013



Memory on Logic

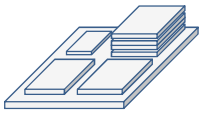


Logic-on-analog

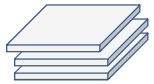


Logic-on-logic (Advanced on Mature)

2015

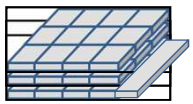


Active interposer (NOC interconnect)



Modular and Stackable processor (NOC interconnect)

Next >2016



Cache memory on many core (3D network-in-memory)

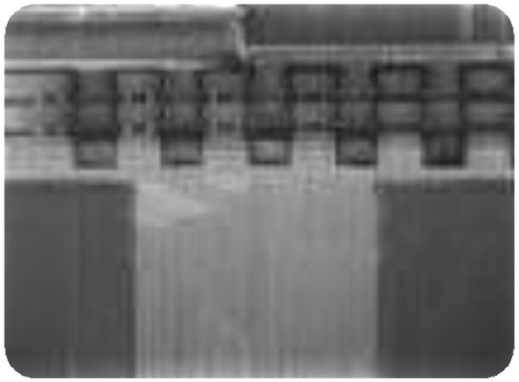
Fine grain partitionning Pitch <10µm

3D Technology Toolbox 200 & 300 mm

Roadmap | 3D TSV vs Monolithic 3D

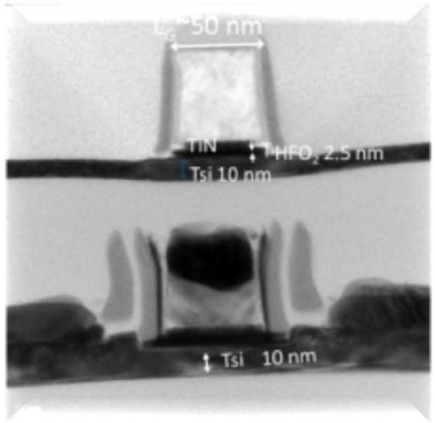
TSV (3D Parallel)

- « back-end » solution
- Mixing of heterogeneous chips (function, node)
- Low-medium density (~um size via, ~10-100um pitch)
- Early introduction as stop-gap and/or low cost



Monolithic (3D Sequential)

- « front end » solution
- Logic-on logic
- Same node on different levels
- Heterogeneous material integration possible (III-V on Ge on Si …)
- Ultimate density (same size and pitch of vias and contact as technology node of application)



Key message: why 3D is changing Semiconductor markets

- The key challenges for future high-end ICs are Yield/Cost, power, data transfer and I/O, Heterogeneous Integration
- 3D is Happening
  - To improve yield , cost and power
  - to shorten distances and increase bandwidth in a single chip, … But off-chip I/O will be the bottleneck. Si-Photonics will be soon required for chip to chip on board and later on Interposer (2.5D)
  - To enable eNVM reducing static power consumption
  - To enable Heterogeneous Integration
- Implications on IC design and then semiconductor markets will be disruptive

Acknowledgement

- Design team: Fabien Clermidy, Denis Dutoit, Marc Belleville, José Luis Gonzalez , Pascal Vivet, Yvain Thonnart
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- Silicon photonics team: Sylvie Menezo, Laurent Fulbert