Road mapping 3D R&D (and I)

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Ireland's EU Structural Funds Programmes 2007 - 2013

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Agenda

- Background
- Heterogeneous Integration
- Possible Applications
- The Opportunities for Innovation
- Conclusions

Europes First 3D Technology (1985)

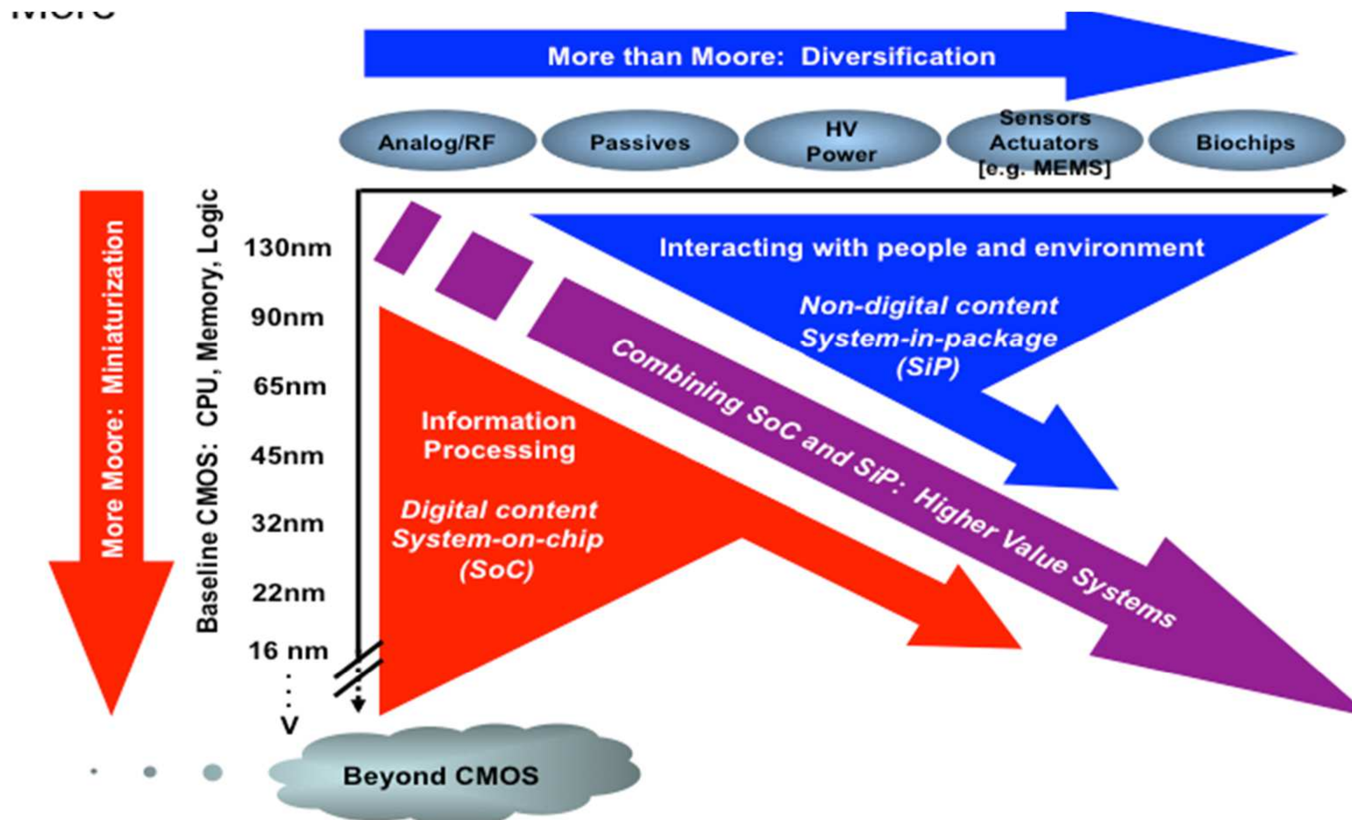
- ESPRIT 245 (3DSOI – 1985-1988)
  - 7 partners
    - STM, CNET, CEA-LETI, Thomson CSF, U. Cambridge, GEC Research, NMRC (Now Tyndall)
- Zone Melting Recrystalization (ZMR) of Si to form single crystal Si on top of SiO2 layers.
    - Laser/ E-Beam ZMR
    - Epitaxial Lateral Overgrowth (ELO) Selective Epitaxial Growth (SEG)
- 3D circuit Evaluation
  - Device Design and Demonstrator

The 3DSOI Consortium

ESPRIT 245 Summary

- Stepper motor controller
  - 'Mezanine' Structure- one layer of interconnect
  - 50-70 V L-DMOS in Bulk, 3um CMOS Gate Array in SOI (40 um Seed window spacing)
  - No thermal impact on DMOS Channel due to ZMR (laser and e-beam) LDMOS channel (<1um)
  - Used SEG and ELO with a-SI to minimize stress at corners of seed layer and planarise structure
- Fully Stacked Inverter
  - No problem for PMOS in bulk due to ZMR Process

Technology Evolution



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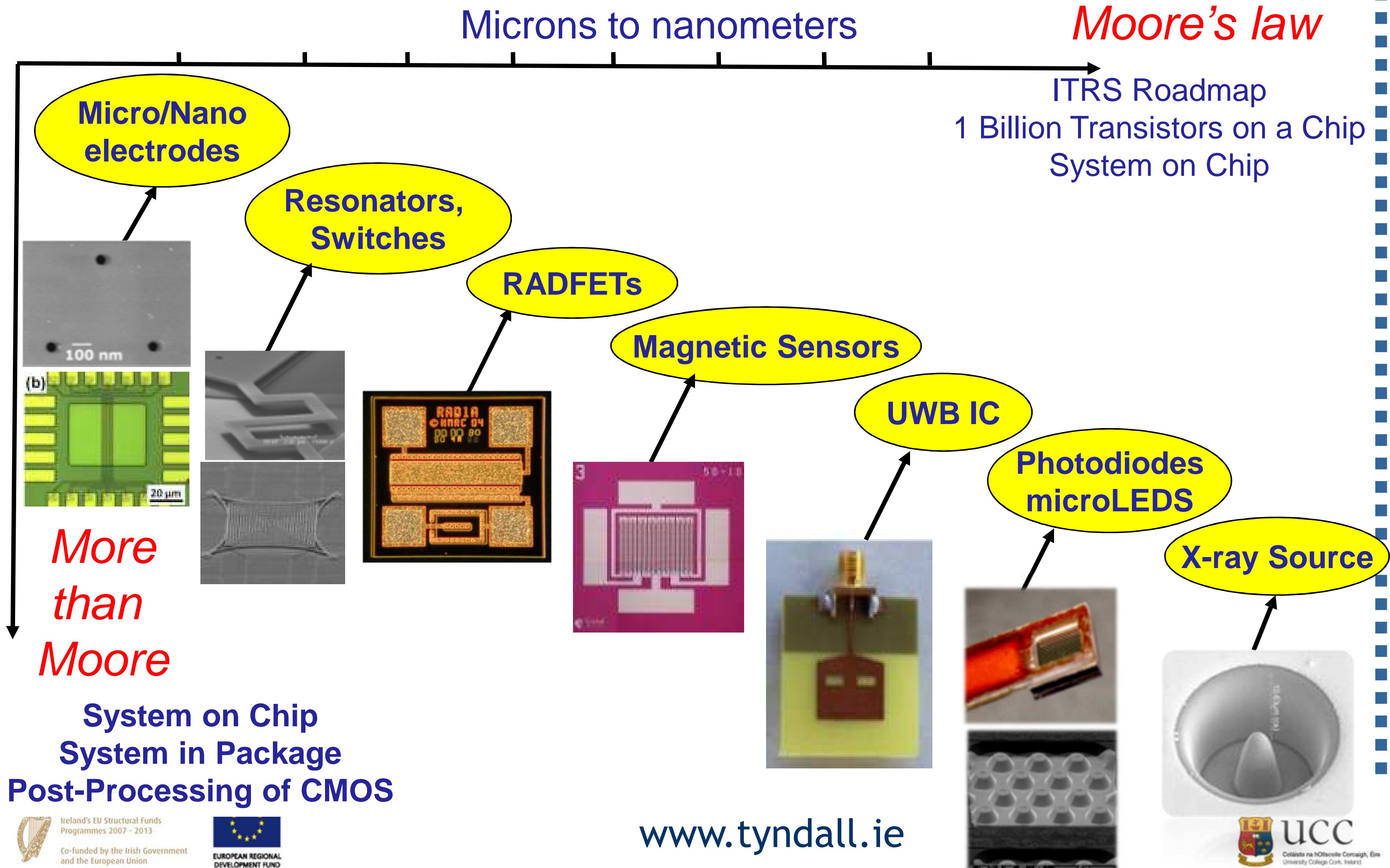
More Moore
- Sensors and Actuators



System on Chip
System in Package
Post-Processing of CMOS

More Moore
- Integrated Energy Solutions

Microns to nanometers

Moore's law

ITRS Roadmap
1 Billion Transistors on a Chip
System on Chip

Energy Harvesting Electromagnetics

Energy Harvesting Piezoelectrics

Thermoelectrics

p-type Bi_2Te_3

n-type Bi_2Te_3

3D Supercapacitors

TiN
Al_2O_3
TiN
AAO
100 nm

Microbatteries

Micro Fuel Cells

More than Moore

System on Chip
System in Package
Post-Processing of CMOS

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ITRS roadmap 3D SIP

This 3D-TSV process is typically integrated in the Si-wafer fabrication line. The 3D-stacking process is generally done outside the standard Si-process line.

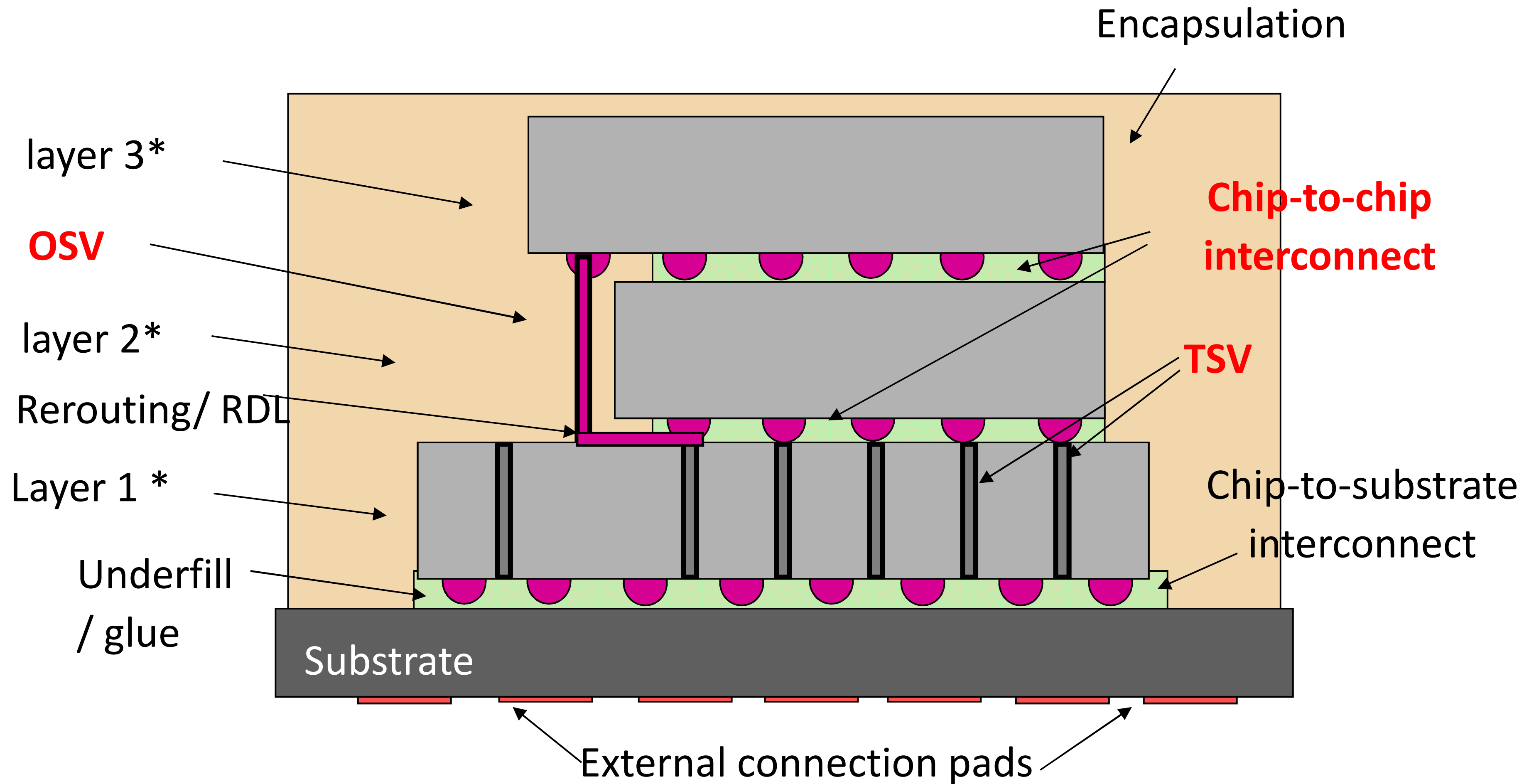
Table INTC7 Global Interconnect Level 3D-SIC/3D-SOC Roadmap Global Level, W2W, D2W or D2D 3D-stacking

	2011-2014	*2015-2018*
Minimum TSV diameter	4-8 µm	2-4µm
Minimum TSV pitch	8-16 µm	4-8 µm
Minimum TSV depth	20-50 µm	20-50 µm
Maximum TSV aspect ratio	5:1 - 10:1	10:1 - 20:1
Number of tiers	2-3	2-4

Table INTC8 Intermediate Interconnect Level 3D-SIC Roadmap Intermediate Level, W2W 3D-stacking

	2011-2014	*2015-2018*
Minimum TSV diameter	1-2 µm	0.8-1.5µm
Minimum TSV pitch	2-4 µm	1.6-3.0 µm
Minimum TSV depth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1 - 10:1	10:1 - 20:1
Number of tiers	2-3	8-16 (DRAM)

Chip Stack Nomenclature



* Stratum / Tier

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TSV Materials issues

Higher aspect ratio fill
- Barrier layer
- Seed layer
- Cu conductor

Significant issues
- Cost
- Speed
- Reliability

- Improved barrier Layer
  - Ability to process in high aspect ratio
  - Plateable?
  - Adhesion
  - Barrier func

- Seed layer
  - Adhesion
  - Conductivity
  - Stability in plating solution

- Cu bottom-up fill
  - On chosen seed/barrier combination
  - High rate
  - Additives required
  - Decrease cost

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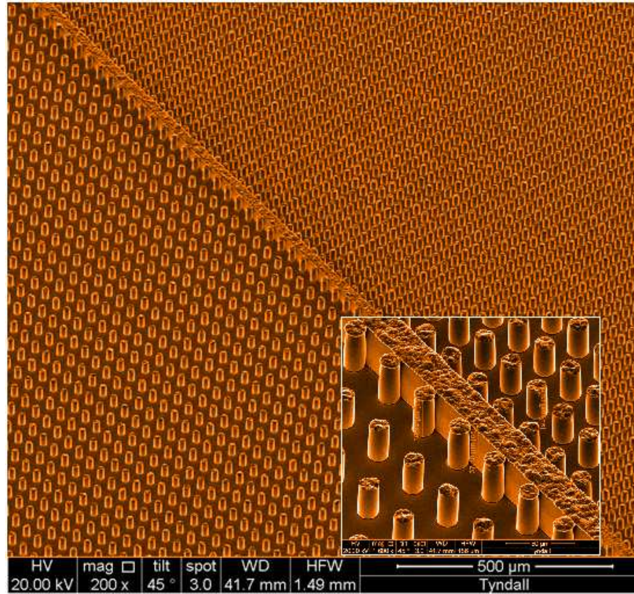
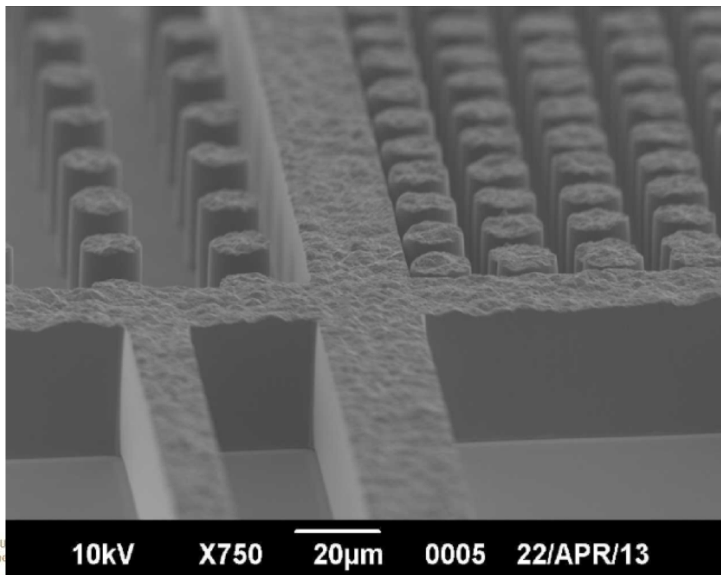
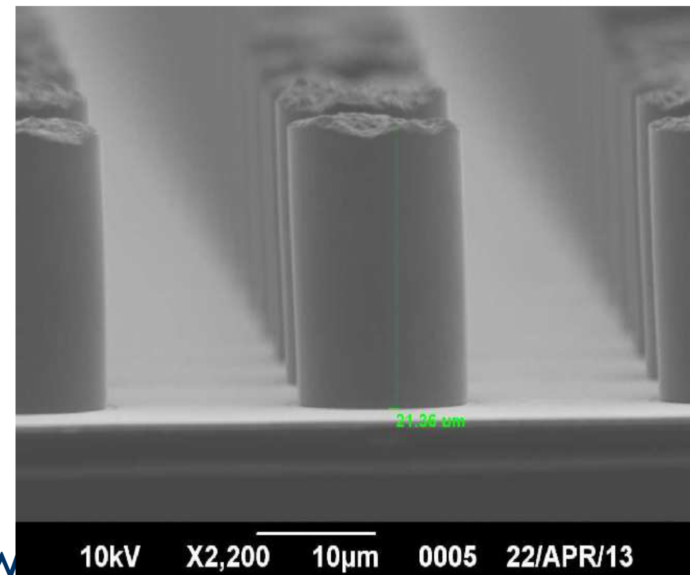
Wafer scale Cu Plating (OSV)

-Cu microstructures in wafer scale deposition using the Digital Matrix wafer plating tool.

-Pillars
-12 μm diameter
-22 μm height.







Low Temperature Interconnect

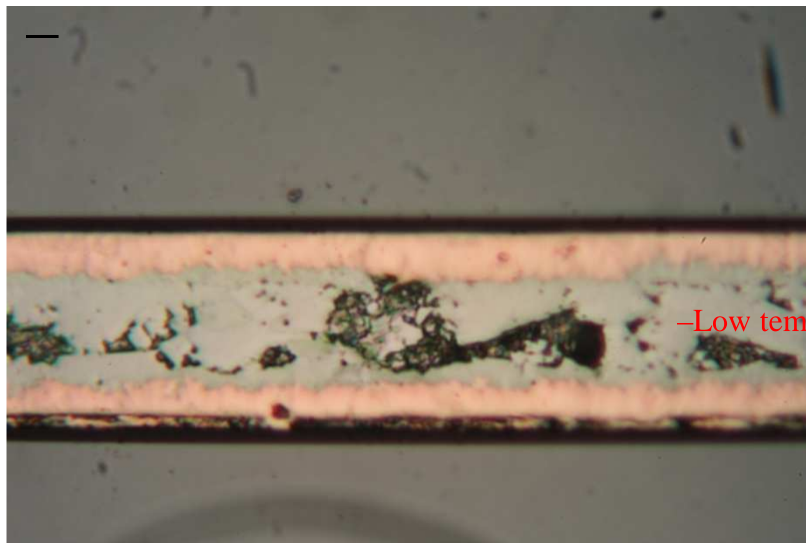
–Attatchment between devices with TSV s need low stress (low temp) bonding

–Low temperature SLID (Solid Liquid Interdiffusion)

– **New research based on multi element compounds to reduce melting point during bonding**

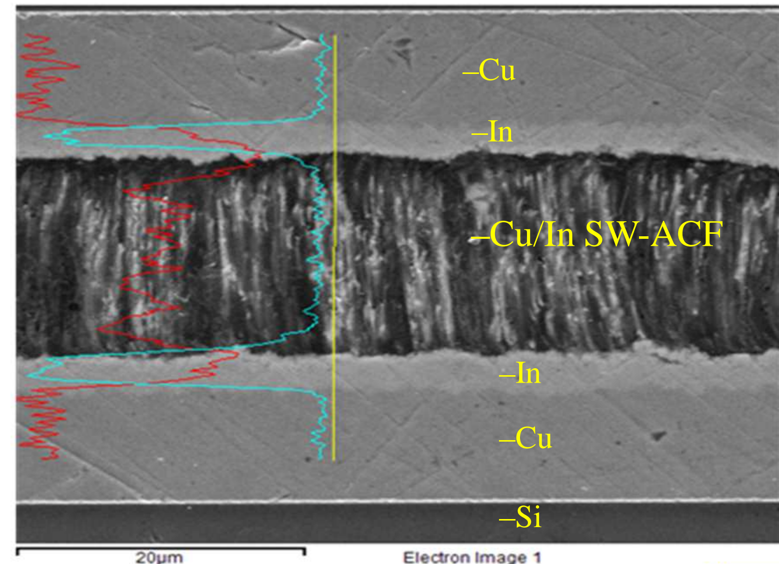
–SW-ACF bonding on In/Cu pads

- **Peak bonding Temperature: 180 °C**
- **Bonding time: 240 s**
- **Bonding pressure: 2.2 N/mm^2**
- **Heat rate: 3 °C/s**
- **Shear testing showed a bond strength of ~7.2 kgf**

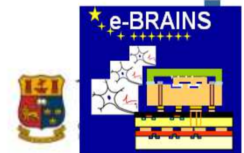


–Optical microscope

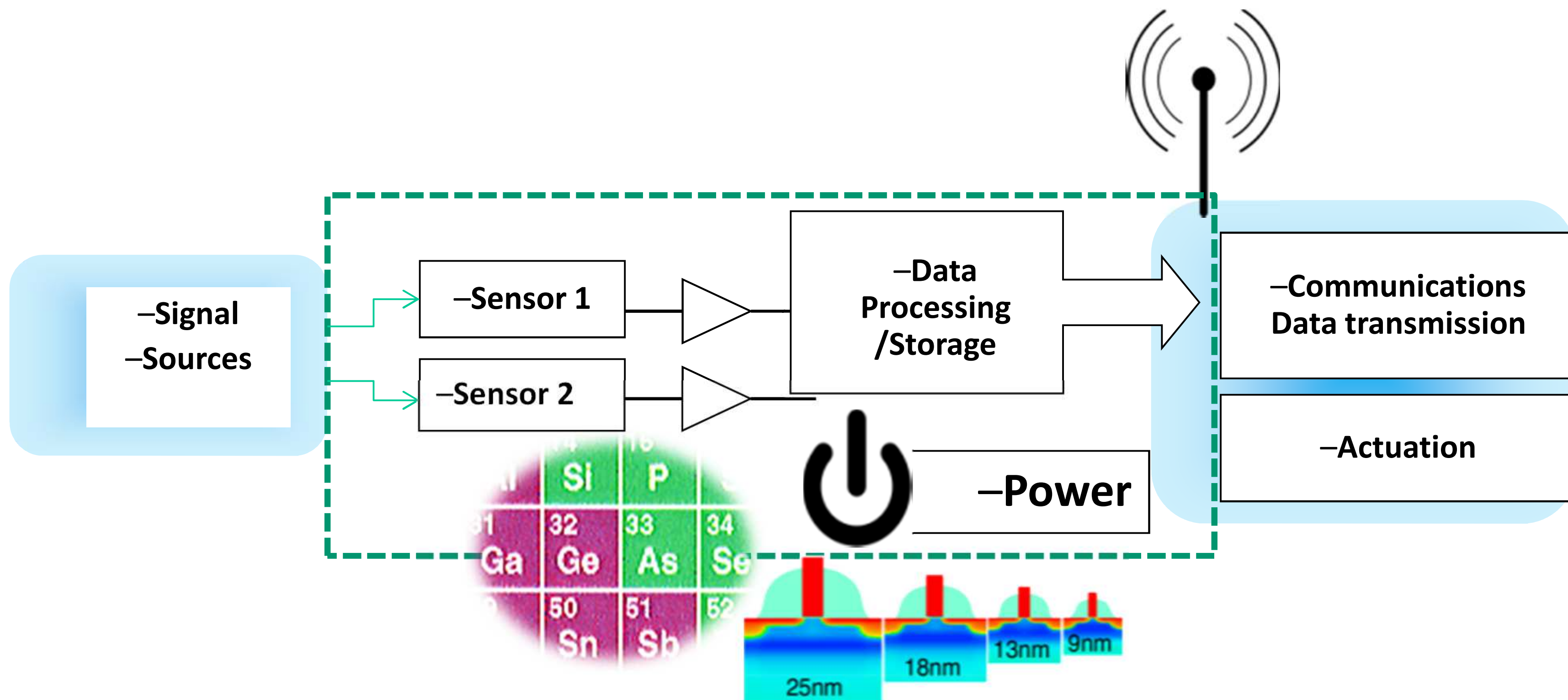
–*Source: Fraunhofer EMFT Muncih*



–SEM and EDX line-scan of Cu/In SWACF bonding interface



Much More Than Moore



Tyndall
National Institute
Institiúid Náisiúnta

SMART Systems - Impacting Society and the Economy

HEALTHCARE:
Longer, healthy lives

COMMUNICATIONS:
Efficient reliable

ENERGY:
Protected, safe, secure

ENVIRONMENT
Sustainable

Tyndall National Institute
Institiúid Náisiúnta

Conclusions

- Europe has extensive expertise in Technologies for More Moore and More than Moore
  - Particularly Suited To Heterogeneous Integration due to broad background in Microsystems
  - Different requirements to More Moore and More than Moore
- RELIABILITY and Process Cost Reduction are the most important items to be studied and big projects are underway to address these issues
  - Reliable and low temperature Interconnect Is very Important
- Sensors Passives, Energy/Power Supply and Antennas are crucial additional capabilities to add to the integrated systems to facilitate autonomous operation
  - All sensors should have TSVs (my opinion)
  - Interposers to be used for system integration
- 3D is Coming Of Age
  - Several research labs are now offering foundry Services for 3D building platforms for the future development of 3D
  - 'Via Last' Is probably the best solution for mixed technology systems