

3D Packaging and Reliability

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Grenoble (France), January 22nd, 2014



■ **Motivation: System Integration Everywhere**

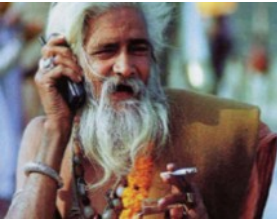
■ **System integration: Packaging makes the Difference**

■ **Success factors**

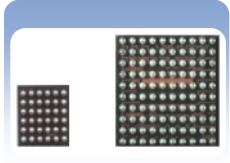
- Understand reliability requirements of customers
- Innovative assembly and packaging technologies
- Understand material physics
- Coherent chip-package-board co-design
- Management of complexity

■ **Conclusions**

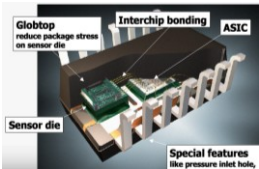
Applications & Customer Requirements SiP integration everywhere



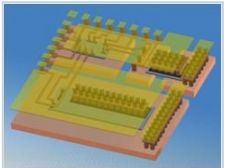
■ Communication and Computing



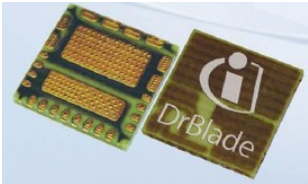
■ Automotive Electronics



■ Energy generation and energy distribution (e.g. smart grid)



■ Industrial Electronics (e.g. energy efficient driver)



■ And others: e.g. Solid State Lighting, medical, aeronautics, ...

Technologies: More Moore is getting out of steam

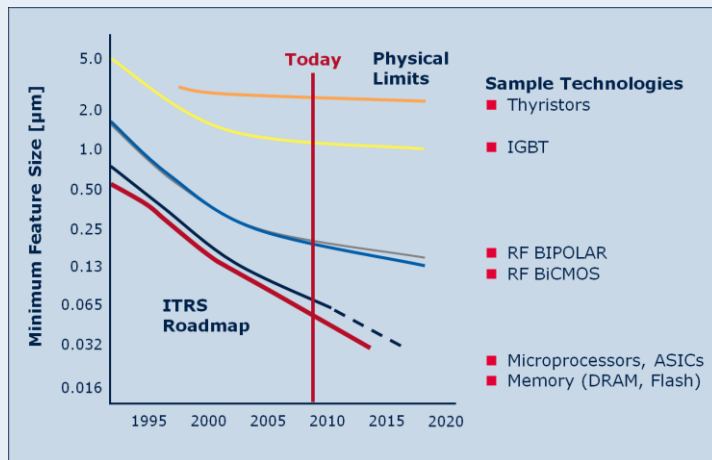
More Moore reaches limits

By shrinking of CMOS

- better performance/speed
- less energy consumption
- miniaturization
- less cost per transistor

In addition:

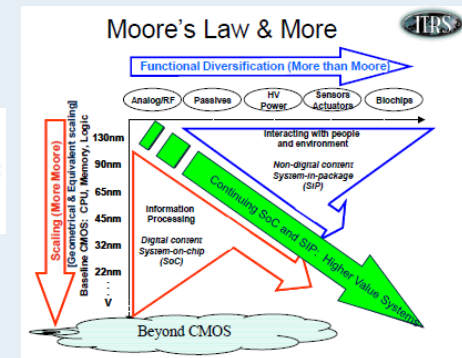
- outstanding yield



“More Moore getting out of steam

More than Moore & High value system

- Packaging has become the limiting element in system cost and performance
- The Assembly and Packaging role is expanding to include system level integration functions.
- As traditional Moore’s law scaling become more difficult innovation in assembly and packaging can take up the slack.



■ Motivation

■ System integration: Packaging makes the Difference

■ Success factors

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■ Conclusions

Innovative packaging makes the difference

■ Example I: Package enables small form factor

■ Example II: Package enables high I/O crossing the interconnect gap

■ Example III: Packaging enables high efficiency

■ Example IV: Packaging enables high performance mm-wave

■ Example V: Packaging enables integration of high functionality



Innovative package allows to overcome barriers

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Reliability: Understand applications and customer requirements



- Different applications have different reliability requirements, e.g. drop test vs. TCoB
- Understand application requirements e.g. checking of board thickness
- It is not guaranteed that the same package fits to different applications
- We need to better understand physics to avoid one chip in different packages
- Different packages have different failure modus; we need to investigate unknown failure modus

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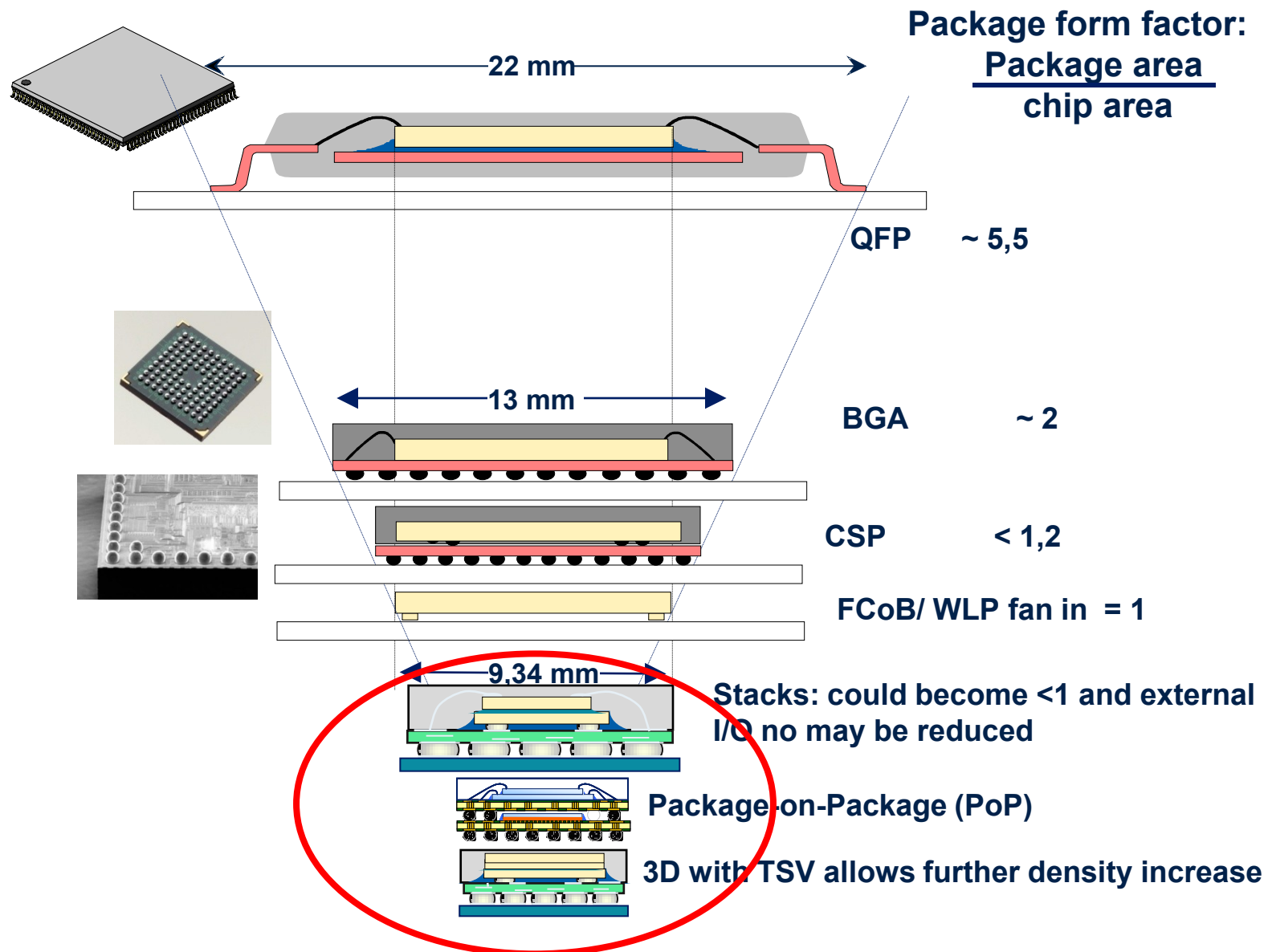
■ System integration: Packaging makes the Difference

■ Success factors

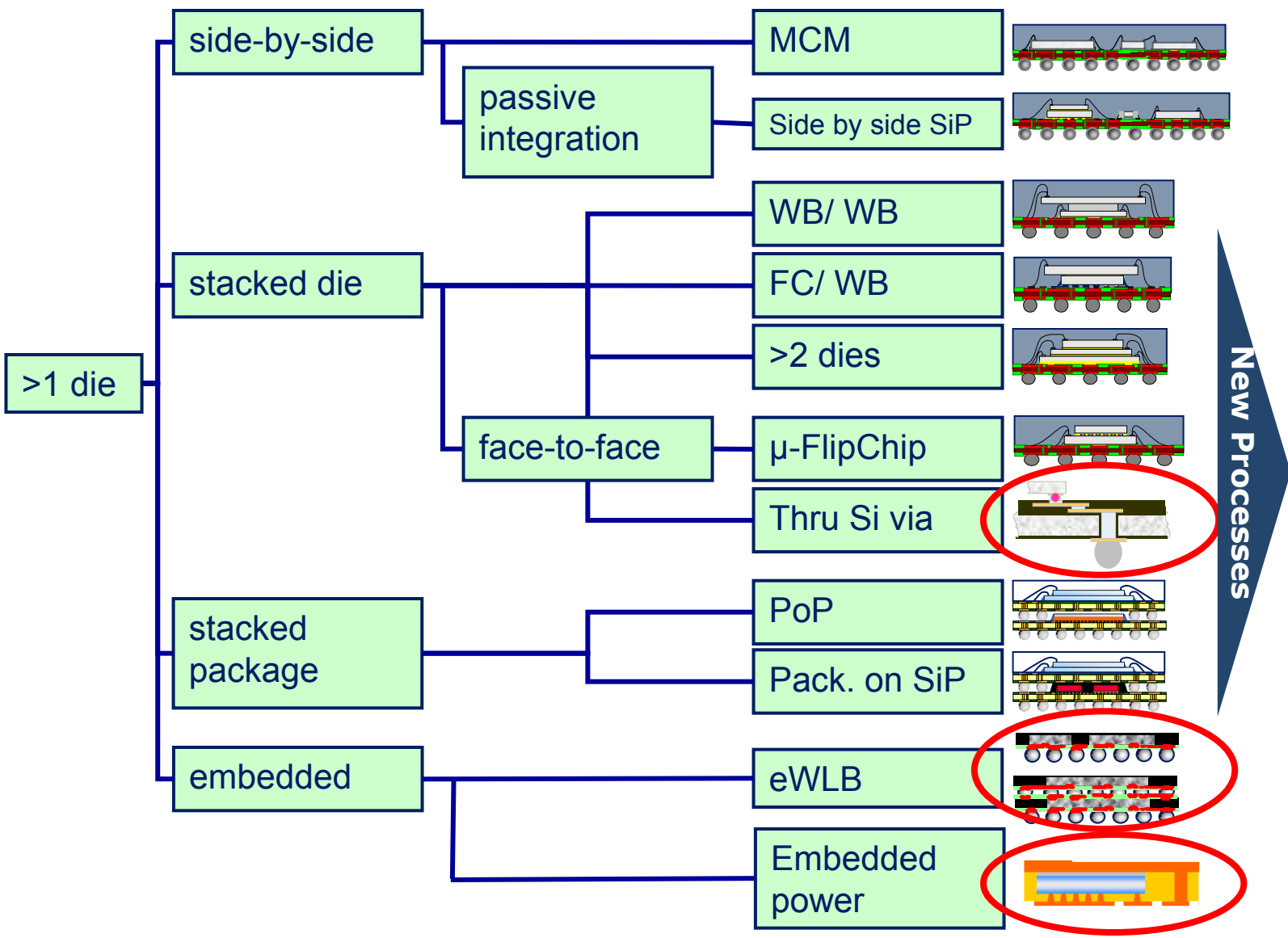
- Understand reliability and requirements of customers
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Miniaturisation and more Functionality require 3D Integration



Examples of BGA based packaging tree - We focus on technologies with low parasitics



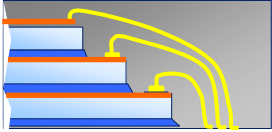
- Wafer level packaging
 - Reconstituted wafers
 - 2.5D & 3D integration
 - Wafer thinning (+ handling thinned wafers)
- Front-end and Back-end merge**

We develop toolbox elements for SiP integration: example: different types of vertical 3D contacts



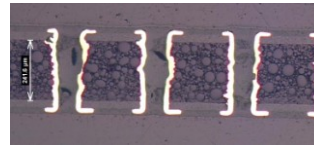
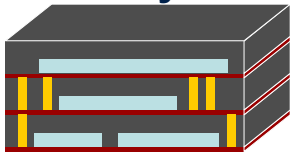
Traditional

3D by Wire Bonding

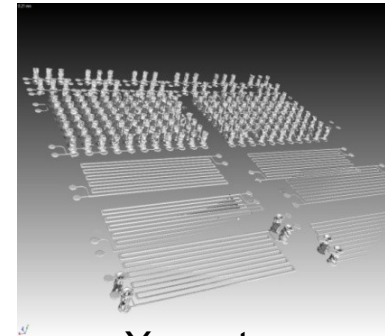


Innovative

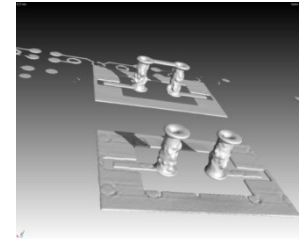
3D by TEV



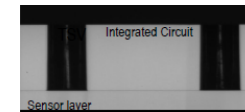
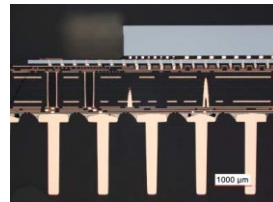
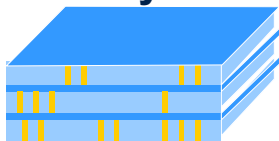
Normal cross section



X-ray tomography

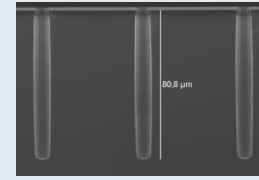


3D by TSV

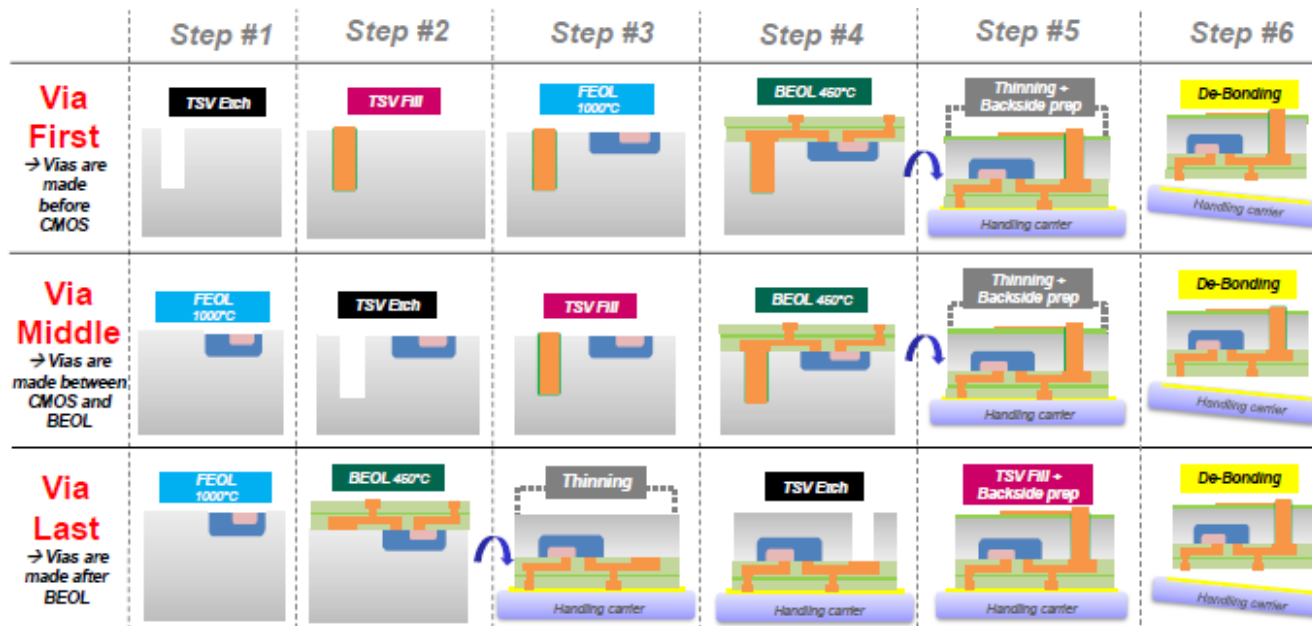


(courtesy of ams AG)

Make the right choice for your toolbox: TSV with (via first), via middle, via last

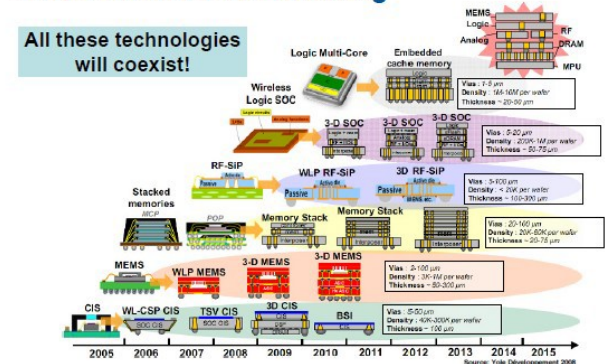


Complexity requires careful technology choice for application

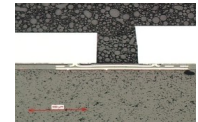
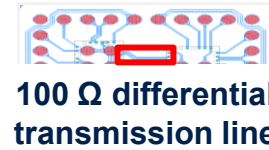


Source: YOLE Developpement 2010
3D IC integration & TSV interconnects

:: Trends for 3D TSV Stacking

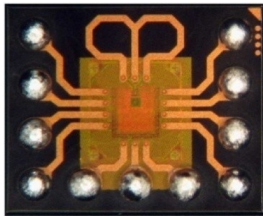


SiP Toolbox elements based on eWLB:

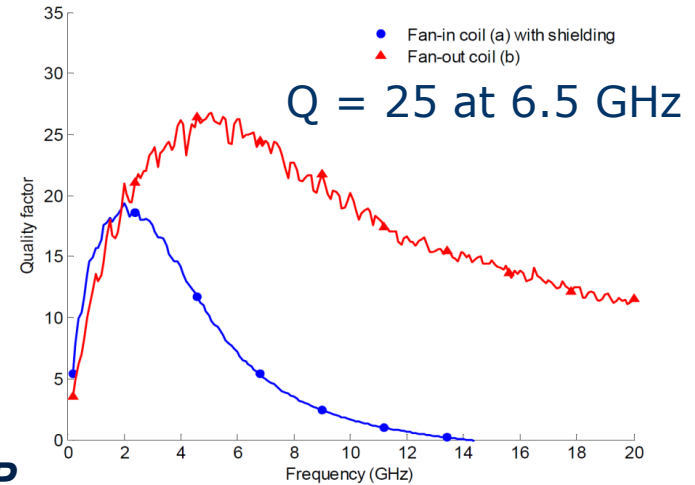
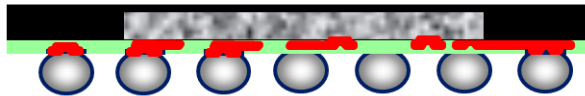


i) Opportunities for side by side connected by RDL

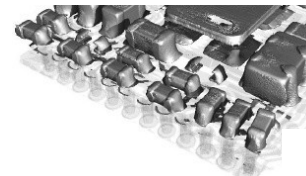
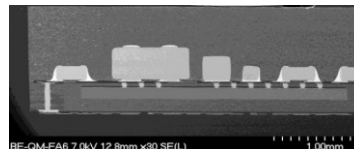
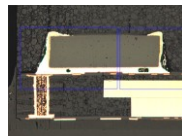
ii) Integration of inductor in fan-out region



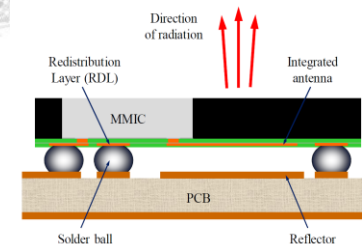
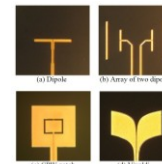
M. Wojnowski et al
(Infineon)
ECTC 2011



iii) Example for 3D integration of discrete passives
(2 dice with stacked & double sided RDL)



iv) Example of integrated antenna
(CATRENE project 3DIM3)



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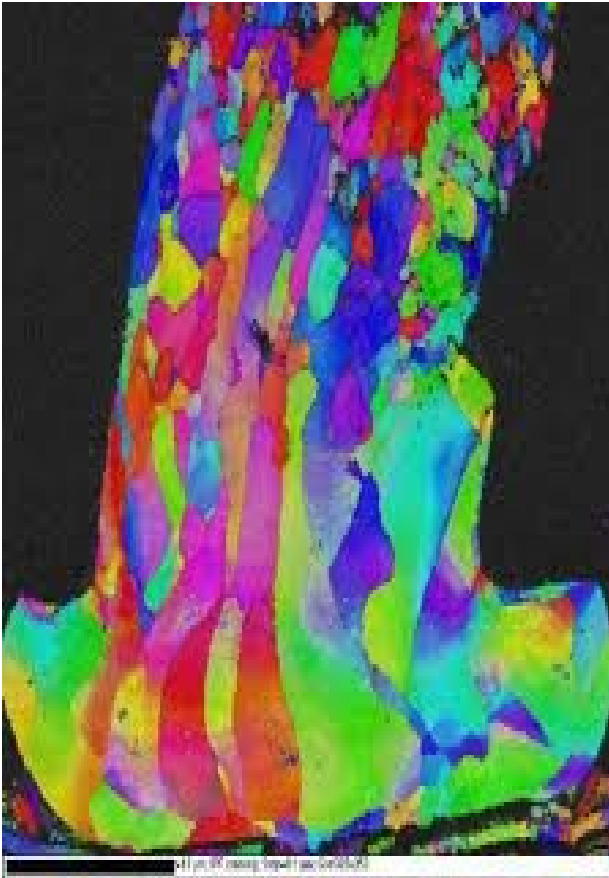
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■ Conclusions

New materials enable package innovations

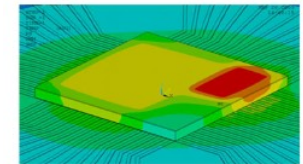
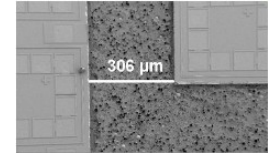
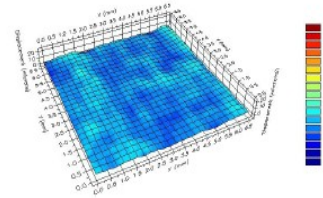


- Dielectrics e.g. isolation for RDL, ...
- Inductors & Caps, e.g. in thin film RDL
- Cu wire,
- Barrier layers e.g. diffusion barrier, ...
- Adhesives e.g. die attach, ...
- Nano-materials e.g. sintering, printing
- Composite materials e.g. advanced mold compound ($> 200^{\circ}\text{C}$)

Success factor: Material Know How

Example for importance of materials in eWLB

- 1) Mold compound with small filler size and low viscosity for side by side SiP (experience from TSLP)
- 2) CTE of materials allows low warpage
=> advantageous for package stacking
- 3) Plating resist and temporary adhesive
- 4) Understand and improve interfaces of materials
(adhesion, avoidance of electromigration, ...)
- 5) Material parameters capable for mm-wave application
- 6) Understand coherence of chip-package-board materials
- 7) Thermal properties =>
design opportunities for hot spots & thermal balls



⇒ Miniaturisation and System Integration with new materials need an advanced failure analysis (FA) capability

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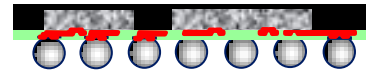
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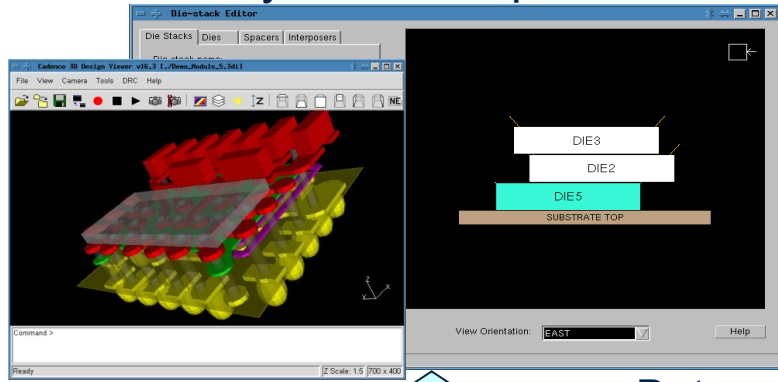
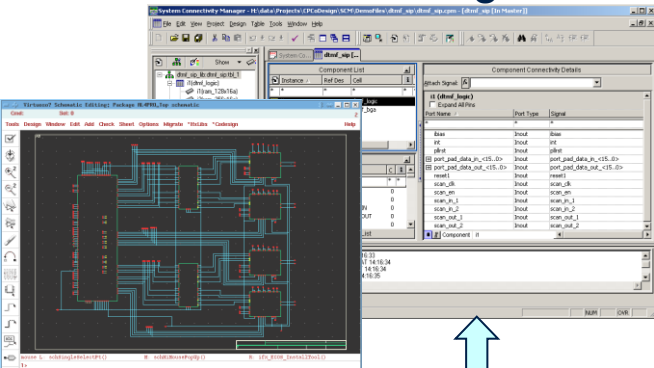
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First work on electrical design & layout in CoSiP project but needs to be extended by multi-physics and more

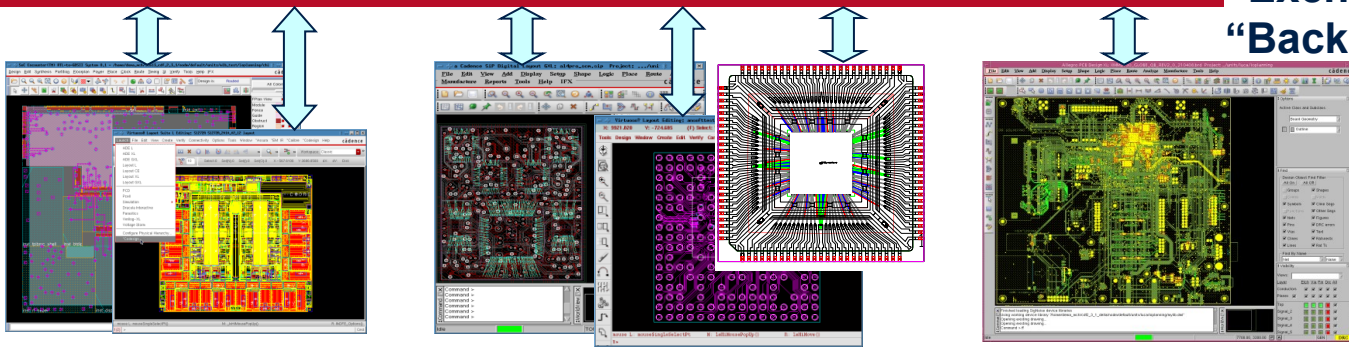


Netlist Manager

System Floorplanner



Data Exchange "Backbone"



Die Design

Package Design

PCB Design

Next steps:
 Implement Multi-physics
 =>
 thermal
 mechanical
 thermo-mechanical
 &
 manufacturability & costs



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Managing Complexity: Summarized we observe 5 trends



■ Demanding system reliability & thermal management

- Expansion towards high reliability applications (automotive, aviation power distribution, medical)
- High reliability of system requires even higher reliability of sub components!

■ Diversity of technology

- Various analog & digital specific IC technologies (memories, RF, processors, power...)
- MEMS (sensors, actuators...)
- Passives

■ Complex material mix

- Wide range of material properties (Si, metal, ceramics, polymers, composites etc.)

■ Convergence of IC/Package/PCB technology

- Wafer level packaging
- Chip embedding in laminate
- Through silicon via & through encapsulant via
- Further shrink of interconnects (fine pitch wire bond, thinfilm technology, TSV)
- Integration of passives or functions in RDL/TSV

■ 3D designs

- Stacked die approaches
- Multiple stacks of sub-packages, interposers...
- PoP (package on package)
- MEMS

Set-up Know How and
investigative standardization

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What do we need?

- Understand your application requirements (reliability)
- Understand your customer (price, performance, ...)
- Understand trade-offs between technologies (TSV, TEV, ...)
- Understand and develop the appropriate toolbox elements
- Understand physics of processes, failures, performance, ...
- Understand your supply chain
-

⇒ **We need T-shaped persons**

⇒ **The EUREKA CATRENE Program opens collaboration opportunities**

