Focus

Application-oriented design technology for micro and nano electronics has become a very important success factor for European micro and nano Electronics companies and will be looked at in its full range. Exhaustive research and development in this area has been supported by CATRENE and ENIAC and local governments through the past years. Latest results and exciting highlights form CATRENE and ENIAC projects will form the subjects of this conference.

Contents

All CATRENE and ENIAC projects related to electronic system design, to design technology and to manufacturing topics are invited to contribute to the conference. Each project may organize a full session made of one tutorial presentation (45 min.) and 2 technical presentations (20 min. each) or contribute to a global session with a tutorial or a technical presentation.

Steering Committee

J. Borel, R&D, France,
B. Candaele, Thales Group, France,
M. Coppola, ST, France,
P. Koch, CATRENE, EU, FhG
Manfred Dietrich , Germany
A. Jerraya, CEA, France,
W. John, SIL, Germany,
Christian Sebeke, Bosch, Germany,
Prof Dr, W. Rosenstiel, Uni. Tuebingen & FZI,
Ralf Pferdmenges, Infineon, Germany,
K. Veelenturf, NXP, Netherlands,
Anne Marie FOUILLIART, Thales Group, France
Petrot TIMA, France,
Jose Calero, DS2,
S Eugenio Villar, Cantabria Univ, Sweden,
Mario Diaz Nava, ST, France,
Mart Coenen, EMC MCC, Netherlands

Preliminary Programme

Wednesday 23rd June

08:45 **Welcome**

09:00 **Opening & Keynotes**

Opening
Laurent Malier, Director of Leti, CEA, France

09:15 **PA representative**
Benoit Formery

09:30 **Keynote :**
Jorgen Lantto, CTO, STE, Sweden

10:00 **Keynote:**
Jean-Marc Chery, CTO ST, France

10:30 **Break**

Technical Session 1 : HW and SW for Multiprocessors and many cores
Chair : Anne-Marie Fouilliart, Thales

11:00 **Tutorial : TSAR Cache-Coherent Architecture**
Prof. Alain Greiner,UPMC, France

11:45 **Specification and Validation of CC protocol**
Huy-Nam Nguyen, BULL, France

12:05 **SoftSOC HDS Architecture**
Marcos Martinez, ES2, Spain

12:30 **Lunch**

Technical Session 2 : Smart Lighting
Chair : Paul Merkus, Philips, Netherlands

14:00 **Tutorial Lighting systems based on Solid-State Lighting devices**
Theo Treuniet, Philips, Netherlands

14:45 **Implementation of LED lighting in a residential show room**
Dominique Persegol; Schneider Electric, France

15:05 **TBD**

15:30 **Break**

16:00 **Panel : ID Security and Biometrics**

Drivers and demand for sophisticated design methods and tools for electronic components embedded software and related systems
Chair : Christian Sebeke, Bosch,
Claude Barral, Gemalto,
Bernard Candaele, Thales,
Claudia Eckert, Fraunhofer SIT,
Detlef Houdeau, Infineon,
Laurent Sourgen, ST,

Technical Session 3 : European EDA SMEs – key for innovation
Chair : Andreas Ripp, MunEDA,

17:30 *Introduction and Overview presentation by Brieuc Turluche, CEO CWS Coupling Wave Solutions and Andreas Ripp CMO & Managing Director, MunEDA*

17:45 **Infiniscale**
Firas Mohamed, President & CEO

17:55 **Edxact S.A.**
Mathias Silvant, CEO

18:05 **Magillem Design Services**
Emmanuel Vaumorin, CEO

18:15 **Panel Session challenges for European EDA SMEs in global markets.**
Moderator : Andreas Ripp, MunEDA,
Panelists :
Peter Feist, CEO Onespin Solution,
Gislain Kaiser, CEO DoceaPower,
Michel Tabusse, CEO Satin-IP,
Brieuc Turluche, CEA CWS Coupling Wave Solutions
Eric Beisser, CEO Xyalis

19:00 **End**

19:30 **Social Event : dinner**

Thursday, 24th June

Keynotes

09:00 **IP & Re-Use – the next wave of a successful model !**
Christoph Heer, VP for Digital IP and Reuse, Infineon, Germany

09:30 **Linking Design and Fabrication technologies**
Michel Brillouet, Fellow, LETI, France

Technical Session 4 : 3D Integration

Chair : Mario Diaz Nava,

10:00 **Tutorial : Present and Future of 3D Integration**
Jean-Marc Yannou, YOLE, France

10:45 **Development of CAD Tools for 3D-Integration**
Heiko Dudek, Jean-Francois Lepere, Cadence

11:05 **Perspectives of Heterogenous Systems using 3D-Integration technology**
Peter Ramm, Fraunhaufer IZM Munich, Germany

11:30 **Lunch + Poster Session**

Technical Session 5 : Low Power Design

Chair : Macello Coppola, ST

14:00 **Tutorial : Power efficient designs form PA and RF to Baseband, from System level to IC implementation**
Bernard Candaele, Thales

14:45 **Top down methodology for SoC power management based on a programmable controller**
Patrick Valdenaire, STE

15:05 **Spidergon STNoC overview, and low power specific features**
Michael Soulie, ST, France

15:30 **Break**

Technical Session 6 : Advanced Test Technologies

Chair : Kees Veelenturf, NXP

16:00 **Tutorial : Test and Dependability of Microsystems**
Serge Bernard, LIRMM and Philippe Cauvet, Ophtimalia, France

16:45 **Evaluation of Parametric Test Metrics for Mixed-signal/RF DFT Solutions using Statistical Techniques",**
Salvador Mir, TIMA

17:05 **Computer-Aided-Test Techniques for the Evaluation of AMS DFT**
Hervé Naudet, STM

17:30 **Closing**

Advance Programme

European Nanoelectronics Design Technology Conference

Highlights form CATRENE and ENIAC projects

DTC

June 23 – 24, 2010

MINATEC®, Grenoble, France
Co-located with MINATEC Crossroads

Chair: Ahmed Jerraya, CEA-LETI, France
Co-Chairs: Mario-Diaz Nava, ST
Denis Rousset, STEricsson,

For More Information:
http://www.minatec-crossroads.com/dtc

For Venue:
http://minatec.congres-scientifique.com/crossroads2010/