Focus

The Design Technology Conference will focus on application-oriented design methods for SoC including heterogeneous functions and SiP integration in themselves a very important success factor for European Micro- and Nano- Electronic companies. Exhaustive research and development in this area has been supported by CATRENE and local governments through the past five years. Latest results and exciting highlights from mainly CATRENE projects will form the subjects of this conference.

Contents

All CATRENE projects related to electronic system design, to design technology and to manufacturing topics are invited to contribute to the conference. Sessions are made of one tutorial presentation (45 min.) and technical presentations (20 min. each).

Steering Committee

Jose Luis Conesa ALPHASIP, E
Bernard Candaele, Thales Group, F
Marcello Coppola, STMicroelectronics, F
Mart Coenen, EMCMCC, NL
Mario Diaz-Nava, STMicroelectronics, F
Manfred Dietrich, FhG, D
Agnes Fritsch, Thales Group, F
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Peter H Koch, CATRENE EU
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Wolfgang Rosenstiel, U. Tuebingen & FZI, D
Juergen Haase, edacentrum, D
Patrick Blouet , ST, F
Martin Barnasconi, NXP, NL
Eugenio Villar, U. Cantabria, E
Christoph Grimm, FhG-UKL D

Advance Programme
Monday 23rd June

08:45 **Welcome Opening**

09:00 **Keynote: Grenoble's innovation Ecosystem, Laurent Malier , CEA Leti**

09:30 **Keynote : Security aware design, Jean Pierre Tual, Gemalto**

10:00 **Keynote : Abelein, Ulrich, AUDI**

10:30 **Break**

Technical Session 1 : Reliability of SoCs in Safety Critical Applications
Chair : Juergen Haase, edacentrum, D

11:00 **Tutorial : "Safety critical systems – How the industry manages to ensure dependability with new microelectronic technologies", Florent Miller, Airbus Group Innovations, F**

11:45 **"Increasing the reliability of SoCs", Vincent HUARD, STMicroelectronics, F**

12:05 **"Designing reliable ICs for automotive applications", Georg Georgakos, Infineon Technologies, D**

12:30 **Lunch**

Technical Session 2 : Power and thermal aware design
Chair: Armand Castillejo ST

14:00 **Tutorial: Coarse Grain Power Reduction at RTL level, Fahim Rahim , Atrenta**

14:45 **Power Mode Selection in FD-SOI Circuits , Edith Beigne / Diego Puschini , LETI**

15:05 **Toward Energy Neutral Operation's Platform , Agnes Fristch TCS & Francois Druilhe STM**

15:30 **Break**

16:00 **Keynote : Evolution and challenges of multimedia in the connected world Laurent Remont, STMicroelectronics**

16:30 **Session 3 Panel : What are the next growth areas in multimedia beyond TV, mobiles phones/tablets, STB , ...? Organizer Mario Diaz-Nava Contributors : ST, Technicolor, Orange, ...**

17:30 **End**

19:30 **Social Event: dinner**

Tuesday, 24th June

08:30 **Keynote** Silicon Europe, Veronique Pequignat, AEPI & Isabelle Guillaume Minalogic

Technical Session 4 : Energy efficient HPC
Chair : F Clermidy, ICT Infrastructure

09:00 Tutorial: Heterogeneous HPC Systems Hu Nam Nguyen, Bull

09:45 DRAM architecture for energy efficiency, Christian Weiss, UKL, (To be confirmed)

10:05 Energy Efficient Server, Denis Dutoit, CEA-LETI

10:30 **Break**

Technical Session 5 : Power Electronics
Chair: Paul Merkus Philips

11:00 The role of power electronics to ever increased energy efficiency
Gerald Deboy, Infineon

11:20 Evolution of the Smart Power technologies and design techniques toward high density in HV applications, Giulio Ricotti, ST

11:40 SOI substrates technology and process challenges to deliver cost competitive industrial substrates that enable increased circuit performance, Manuel Sellier, Soitec

12:05 High efficiency High Voltage to Low Voltage DC/DC Converter for electrical or hybrid vehicle, Patrick Dubus, Valeo

12:30 **Lunch**

Technical Session 6 : Design enablement for advanced silicon technologies ,
Chair: Ahmed Jerraya CEATech

14:00 Tutorial: FDSOI technology for energy efficient SoC, Gergio Cesana, ST

14:45 Advanced process enablement; Gerd Teppe Global Founderies (To be Confirmed)

15:05 "Advanced System Design Enablement, Patrick Blouet ST, Agnes Fritsch, Thales

15:30 **Break**

16:00 Session 6 Panel: EDA beyond IC design
Chair : JM Chateau, ST
Contributors : Synopsys, Atrenta, Mentor, Cadence, Magillem, Doceapower

17:30 **Closing**

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MINATEC®, Grenoble, France

Chairs: Ahmed Jerraya, CEATech, France
Co-Chairs: Marcello Coppola, ST
Patrick Blouet, ST

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