Use formal, online communication to deliver design quality closure

Stéphane Bonniol

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If an integrated circuit design is to meet the need for high-quality/low-risk implementation, the need for formal communication among the participants in the design process is obviously necessary. When design engineers, design managers and mask shop engineers are at multiple sites--each team and each site working within their own schedule constraints--moving communication online is a must.

Online communication lets system-on-chip integrators do their jobs in parallel to intellectual property design and software development, and in complete awareness of the design-for-mask-manufacturing (DFFM) constraints imposed by the next engineering steps.

IP designers, for instance, need to communicate where they stand with respect to predefined quality criteria (such as functionality, performance and reusability). Regardless of their position in the design chain, engineering and design managers now spend 20 to 40 percent of their time compiling quality progress reports based on individual, manual reports. Although quality standards are available, and most large companies have strong in-house experience managing quality, reporting is still largely ad hoc, Excel-based and manual.

A more formal understanding of what constitutes design quality, and an automated, online method for designers to check quality run after run, dramatically reduces quality reporting time.

Formal, online communication is also a must for mask shop engineers. Stopping any mask during mask processing requires a waiver from the customer and will add a delay of 12 to 24 hours to its delivery schedule, depending on the stage during which the problem is detected. Since such quality issues are usually discovered very late in the process, on items that often have passed normal inspection, they can delay the entire project by a month or more.

Photomasks could be manufactured at lower risk and with higher productivity if design engineers followed specific, well-defined practices before delivering GDSII tapes. Automating these practices and making information available online to all members of the design chain allows monitoring so that DFMM parameters can be fed back from mask manufacturing to designers.

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Successful project management

Online communication not only is a must for technological reasons but is also vital to successful project management. Design, mask making and process engineering have always seen themselves as separate areas, dependent on sets of rules that isolate them from one another's technology. The ever-increasing number and complexity of design rules, however, make the traditional, isolated design paradigm unsupportable.

Engineering management and designers all need to set up design reviews with a higher level of formalism, but the data must be objective; automatically generated; available to all team members concurrently; and based on in-house quality metrics, in addition to external standards, in order to be widely accepted and deployed. Quality status reports that are "correct by construction," that eliminate errors introduced by human interpretation and that are simple to read make it easier to understand issues and take corrective action.

A method to implement close interaction among the manufacturing, mask and design communities exists today. Design quality closure, which can be defined as the condition of passing an acceptable subset of predefined quality checks for safe handover to the next engineering team, can be applied automatically to all steps of a chip design process. DQC's characteristics are reuse of quality standards when available, openness to user specifics, and opportunity to formalize and deploy new quality rules over time.

VIP Lane from Satin IP is a DQC solution that helps companies set up their design methodologies by importing prewritten design quality checks. The Home Entertainment and Display (HED) group at STMicroelectronics uses VIP Lane to let members of the design team extract and present quality metrics with one click. The DQC solution extracts data from the HED IP design flow to allow detailed monitoring of IP quality during the development cycle, automatically produce IP integration documents at delivery time, and consolidate IP quality metrics for an SoC's IP set.

Quality standards for internally developed synthesizable IP had been in place within the STMicroelectronics HED for more than 10 years, culminating in automation of the full design flow, from RTL to gates. Using the online communication and collaboration capabilities of VIP Lane, the STMicroelectronics HED group formalized 110 quality checks and design metrics by consensus among designers, tool specialists and methodology experts. Then, using the DQC tool, it developed 205 relevant sensors for data capture from about 140 design flow artifacts, and wrote formulas for data combination and shaping.

With those in place, extracting the metrics and creating the IP integration document with the DQC tool takes less than 5 minutes. The automatic generation of the IP integration document saves one day per IP iteration and lowers the risk of subjective interpretation. For a design of 20 IP blocks, with an average of 15 iterations per block, the savings can amount to 300 days per design.

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Design practices

Methodology is nothing if it's not deployed. In DFMM, the challenge is twofold: Design practices have to be formalized so that design engineers become more "DFMM aware," and those practices must be used proactively, based on real mask shop-level parameters, rather than simply being documented and then ignored. Adopting online communication as the norm at the same time as practices are formalized greatly increases adoption and compliance by global team members.

Industry initiatives such as the European Crystal collaborative research and development program are intended to significantly improve DFMM by identifying and formalizing recommended design practices to make mask manufacturing a more efficient and less iterative process. While the old design rule checkers (DRCs) developed into sophisticated and proactive design-for-manufacturing tool suites, mask rule checks are still implemented at the final phase, when the GDSII data is released. Resolution enhancement techniques and optical proximity correction further restrict the ability to revise the design or even to take into account the mask manufacturability issues for an additional design cycle.

Crystal's goal is to help improve design consistency, on-time delivery and the cost of photomask design by providing online, real-time access to real data about the manufacturing challenges at mask shops and about the design practices in the upstream design phases that could solve those challenges. Such initiatives also align the development and availability of the real-time data points to the need for leading-edge design quality check libraries in addition to the standard libraries.

One of the Crystal work packages is devoted to identification and formalization of recommended design practices to make mask manufacturing more efficient. Crystal will also provide the tools to deploy and monitor those practices throughout the design chain, a process greatly enhanced by online collaboration among chip design teams, semiconductor fabs, mask shops and EDA vendors.

Crystal is sponsored by the Cluster for Application and Technology Research in Europe on Nanoelectronics (CATRENE). Participants include Atmel, CEA-LETI, Satin IP Technologies, Toppan Photomasks France and Xyalis.

Today, close interaction among the manufacturing, mask and design communities is key to successful product development. A formalized design quality closure methodology, with technology deployed through a secure Internet connection, enables multisite development teams to improve design productivity and significantly reduce risk.

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