EE Times europe
Global news for the creators of technology
APPLY NOW FOR A FREE SUBSCRIPTION

EETimes europe DesignLine
Platinum Sponsors:
freescale

Technical Papers

Strukturierte ASICs der zweiten Generation lösen zunehmend FPGAs ab

Nextreme Structured ASICs

UML for C

Catrene opens for next round of project proposals

John Walko
EE Times Europe
01/22/2009 1:17 PM

Print
Email
Reprints
SHARE

LONDON — Europe's Catrene program, the follow on R&D initiative to take electronics into the nanoscale era, has put out a further call for project proposals, and small to medium sized companies, research organizations and academic institutions have until April 30th 2009 to submit proposals.

Catrene (Cluster for Application and Technology Research in Europe on NanoElectronics), is a four-year program, set to operate under the auspices of the Eureka program and started on Jan. 1 2008.

It is earmarked to make use of 4,000 person-years of effort each year, equivalent to about 6 billion euro for the extended program, which builds on set to build on Medea+ and its predecessors Medea and Jessi.

Commercial participants in Eureka projects can usually get half their costs paid by their national governments while academic institutions can get up to 75 percent of their costs paid.

The first phase of the research initiative involves 12 projects that resulted from the first call last year, and involves 4,000 researchers in 140 organizations from 13 countries.

This second call opens on March 2nd, and project labelling is planned for the end of September 2009. Chosen projects will likely commence January 2010.

The program's main aim is to work on achieving leading positions for Europe in a number of key applications

CAREER CENTER

Work - right now, just another four letter v
Open | Close

RELATED ARTICLES

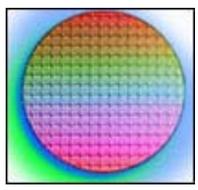
- Analysis: Intel could kill two birds with one F
- Intel forms Intel Labs Europe with hubs in D
- Finland poured $677M into R&D last year
- Czech Republic sees FDI drop off
- 3S Photonics diversifie son activité hors de

Around EE Times Europe

Qimonda files for in
DRAM maker Qimo for insolvency at a M The bail-out negotia financing package c completed in time, t said.

CEO interview: with Wierenga of Philips
The boss of Philips considers the best v in a variety of areas Philips is still active

ST carrying the torc
STMicroelectronics as the most likely b Europe's multiyear a rapidly accelerating of the regional high-



450-mm fab debate
The 450-mm wafer debate surfaced at Strategy Symposiur Half-Moon Bay, Cal

Eight resolutions fo
In order to survive t year, companies ne their way of thinking embrace new ideas concepts, according Penn, CEO of Futur

Gartner's 2008 top t
Gartner sees falls i chip market in both 2009. Here can be market researcher's ranking chart accor preliminary results.

All White Papers »

areas.

It has defined several headline projects, dubbed 'Lighthouse Projects' which address major socioeconomic needs such as transportation, healthcare, security, energy and entertainment through focused R&D programs.

Related Articles:

Catrene opens up for first proposals

Brussels forum plans to lobby EU for chip industry support
Catrene names ex-Infineon exec as VP

Print
Email
Reprints
SHARE

Podcasts
Interview With Bruce Powel Douglass: What Is Agile?

POLL
How do you think R&D spending will fare in 2009?
R&D spending will broaden and speed up
It will intensify, narrow the focus
No different to previous years
Market exits means there's less need to spend
There's less money to spend and it must be made to last longer
From now on many firms won't be doing R&D, they will buy it in
Vote
Visit The Poll Archives

Top 20 chip supplie
Six of the top 10 ch
are expected to suf
declines in 2008, wi
broader industry ha
'annus horribilis' for
chip segment.

Silicon 60 version 7
The EE Times 60 E
Startups list, first pu
April 2004, has bee
version 7.0 to reflec
corporate, commer
technology and mar
conditions.

HOME | ABOUT | CONTACT | FEEDBACK | RSS | NEWSLETTER | MEDIA KIT | CALENDAR OF EVENTS | SUBSCRIPTIONS | NEWS

NETWORK WEBSITES

Green SupplyLine | CommsDesign | DeepChip.com | Design & Reuse | Embedded.com | Embedded Edge Magazine | Embedded Computing Solu Analog | eeProductCenter | Electronics Supply & Manufacturing | Inside [DSP] | Automotive DesignLine | Power Management DesignLine | W DesignLine | Video/Imaging DesignLine | Industrial Control DesignLine | Programmable Logic DesignLine | Audio DesignLine | Mobile Handset D TechOnLine | DSP DesignLine | EDA DesignLine | RF DesignLine | Digital Home DesignLine

INTERNATIONAL

EE Times | EE Times JAPAN | EE Times Asia | EE Times CHINA | EE Times FRANCE | EE Times GERMANY | EE Times Korea | EE Times T Times UK
Electronics Supply & Manufacturing - China | Microwave Engineering Europe | Analog Designline Europe | Industrial Designline Europ Automotive Designline Europe | Power Management Designline Europe | Embedded-europe.com | Mechanical Design

NETWORK FEATURES

Career Center | Conference/Events | Custom Magazines | EE Times Info/Reader Service
NetSeminar Services | Sponsor Products | Subscribe to Print | Global Supply Chain Summit | Product Shopper| ProductCasts | Reprints | EDA

China PCB - Low Cost
Quality prototype to production Instant price, check online! www.pcbcart.com

Ads by

All materials on this site Copyright © 2009 TechInsights, a Division of United Business Media LLC., EETimes EU Copyright All rights rese
Privacy Statement | Terms of Service