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Ex-ST exec calls for EDA to take strategic view

[Anne-Francoise Pele](#)
[EDA DesignLine](#)
 01/20/2010 9:04 PM

PARIS — When asked if the EDA industry has a roadmap, Joseph Borel, ex-executive vice president in central R&D at STMicroelectronics NV (Switzerland, Geneva), answers affirmatively as Europe continually renews the Medea+ EDA roadmap. The real question should however be: Does the EDA industry need an international roadmap?

Writing in [an article](#) on *EDA DesignLine*, Borel argued for an international EDA roadmap. As Moore's Law splinters and new approaches such as TSV gain credibility, he said it's time for EDA to move to a more open approach in terms of sharing the definition of priorities and sharing strategic developments requested by users. It's time for EDA to adopt a more productive approach.

The publication of the article began with a discussion between Borel and *EDA DesignLine*.

"Does the EDA industry have a roadmap? My answer to this question is definitely YES," emphasized Borel, now at the JB-R&D EDA consulting company. "Europe has an EDA roadmap, and has had it for several years within European programs, established on my initiative, under my responsibilities and in collaboration with all European players."

Indeed, Europe has been in a continuous EDA roadmapping process with the definition of its annual

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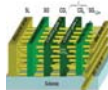
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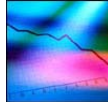
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Memory to rise to 3-D challenges
 The semiconductor memory industry is about to experience major technological changes as three-dimensional multi-gate structures push transistors and memory architectures forward, according to a one-day memory workshop held last month in Grenoble, France, by leading researchers from around the world.


Startup rewrites NXP's legacy in 3D passive integration
 Economic crises can have positive as well as negative impacts. Thus, if NXP had not divested its wireless business and decided to sell its integrated passives device unit near Caen, Normandy (France), Ipdia would not have emerged with an ambition to deliver next-generation 3D-SiP modules for various applications, including advanced LED modules.


Forte chute du marché français des puces en 2008
 Le Syndicat des Industries de micro et nanotechnologies, plus communément appelé Sitelesc, présente un triste bilan pour l'année 2008. Le marché français des semi-conducteurs a chuté de 16,8%, de 2 722 millions d'euros de chiffre d'affaires en 2007 à 1 693 millions d'euros en 2008.

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For those of you involved in embedded systems development: which of the following types of operating system are you planning to use in your next project?

- In-house developed OS
- Commercial proprietary
- Linux
- Android
- My project doesn't need an OS

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global R&D programs.

"Europe is ahead in terms of EDA roadmapping. This may be explained by the fact that EDA business remains small in Europe, and also because US companies tend to acquire our startups' accomplishments. It is high time that we change this situation with the advent of new technology approaches such as TSV."

Borel attracted the attention on [The European EDA Roadmap 2009](#), a 352-page document that he and twenty European industry and R&D contributors wrote for the timeframe 2008 to 2013.

In more specific terms, *The 2009 European Roadmap for design automation in semiconductor products* describes mainly SoC and SiP products, taking the best of technology capabilities for addressing new markets. The 2009 edition mainly focuses on demonstrating a complete top-down design flow, starting at specifications, then system level Design linking designers to formal customer's specification, parametrizable IPs creation, standards and Design for Manufacturability (DfM) supported by new TCAD (Technology CAD) developments.

Published mid-2009, the document is revised and expanded with new ideas, notably CAD linked to Design for Manufacturability (DfM), Systems in a Package (SiP) using new technology approaches such as TSV or Through Substrate Vias for 3D stacking), security and reliability (Dependability), every year.

Borel indicated that Chinese contacts called for the translation of the European EDA Roadmap 2009 in their language.

Page 2: [Ex-ST exec calls for EDA to take strategic view](#)

Page 1 [2](#)

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[Choisir un processeur faible consommation adapté à votre projet de conception](#)

Auparavant, pour concevoir un CPU faible consommation, il fallait faire des concessions sur les fonctionnalités, abaisser la fréquence d'horloge, ou encore attendre l'arrivée de nouvelles technologies permettant de réduire la consommation d'énergie nécessaire en mode veille comme en mode actif. Aujourd'hui, ce n'est plus le cas : le monde des processeurs a subi des transformations radicales.



[Convergence power multi-corner multi-mode : une nouvelle dimension pour la conception des circuits intégrés](#)

S'il est si délicat de franchir la limite des 65-nm pour produire des circuits intégrés, c'est parce qu'il est extrêmement difficile de gérer efficacement la consommation associée.



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Le numérique et l'analogique sont omniprésents. Mais quelle est la différence entre un CNA R-2R et un CNA à chaîne de résistances ?

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