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The aim of the work is to combine the design of silicon, chip package and the board or substra within the SiP into a single design flow

The hope is this will introduce the types of efficiencies that are already seen in the design of So devices

The four company partners are funding about 50% of the CoSiP research project which is co-ft by the German Federal Ministry of Education and Research (BMBF), is due to be completed b end of 2012.

The project work is being carried out in close cooperation with the European MEDEA+ project "Chip/Package-System Co-Design - An Enabler for Compact System-in-Package Solutions".



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