

Research

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Process R&D

ST to create 650 jobs and spend \$1.25bn at Crolles

by **David Manners**

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STMicroelectronics will create 650 jobs and invest \$1.25bn in the **Crolles** R&D and wafer fab facility by 2012, according to ST's CEO, Carlo Bozotti, who added that the investment would give ST 'strategic independence'.

Bozotti was speaking at a ceremony to mark the formal launch of **Nano2012** a joint R&D programme with CEA-LETI, the French Laboratory for Electronics & Information The French Minister of Economy, Industry and Employment, Christine Lagarde, said the investment was: "Strategically important since we will be keep a French production site in a sector which is absolutely crucial for us."

Nano2012 is a public/private strategic R&D program, led by ST, which gathers research institutes and industrial partners and is supported by French national, regional and local authorities.

The Nano2012 cooperation programme, with other programmes such as CATRENE, aims to provide will Europe's electronics industry with competitive access to the most advanced CMOS technologies from 32nm down to 22nm.

Work on the Nano2012 programme started on January 1, 2008. The five-year program, which will run until December 31, 2012, is partly funded to the extent of Euros 457m by the French public authorities.

Other partners are INRIA (the French National Institute for Research in Computer Science and Control), CNRS (National centre for Scientific Research), universities, and many small- and medium-sized enterprise partners.

ST and CEA-LETI initially set up of the Crolles R&D centre in 1992, with CEA-LETI providing the interface between long-term academic research and ST's market-driven industrial R&D.

In July 2007, ST joined the semiconductor Joint Development Alliance centred at IBM's Semiconductor Research and Development centre in East Fishkill and Albany, New York, which develops core and low-power CMOS processes from 32 to 22nm, and IBM joined ST in Crolles to develop value-added application-specific derivative CMOS technologies.

CEA-LETI and IBM, which have complementary expertise in the development of materials and processes required for CMOS technology, are collaborating on advanced process R&D down to 22nm and beyond, at CEA-LETI's Grenoble site (France), IBM's East Fishkill facility (NY), ST's Crolles site (France), and at the Albany NanoTech research centre (NY).

Since the start of the Nano2012 program in January 2008, ST and IBM have exchanged researchers between their sites at Crolles and East Fishkill and have begun working along with researchers from CEA-LETI on a variety of key programs, including 32nm and 28nm core CMOS processes, 45nm RF (Radio Frequency) derivative technology for wireless applications and 65nm non-volatile-memory derivative technology for use in automotive and smart-card applications.

Nano2012 focuses on technology platform development for low-power and application-specific derivative CMOS technologies. A technology platform encompasses the manufacturing process by which billions of transistors are integrated onto a single silicon chip as well as the components libraries and the design methodology to efficiently design leading-edge circuits in this process.

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