Von unseren Partnern im Ausland

Aeneas

MASP 2010
Multi Annual Strategic Plan

The Multi Annual Strategic Plan – also called as MASP – of the ENIAC Joint Undertaking (JU) will enable researchers of the nanoelectronic community to plan their R&D project in accordance with the ENIAC calls for the next 3 years.

MASP is intended to describe the target markets, technical challenges and plans for implementation together with a view of what may be funded for the next 5 years.

MASP connects the Strategic Research Agenda (SRA) of ENIAC with the Annual Work Programme (AWP).

The edaWorkshop09 and CATRENE/MEDEA+ DTC will give all experts the opportunity to contribute their valuable requirements.

Abbildung 4.01: The announcement of the MASP 2010

For more information about European Nanoelectronics Initiative Advisory Council (ENIAC) see http://www.eniac. eu/index.php

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edacentrum started to update the MASP for 2010 at the edaWorkshop09

The Multi Annual Strategic Plan – also referred to as MASP – of the ENIAC Joint Undertaking (JU) and its organisational body AENEAS will enable researchers of the nanoelectronic community to plan their R&D project in line with the ENIAC calls for the next 3–5 years. MASP is intended to describe the target markets, technical challenges and the plan for implementation together with a view on what may be funded for the next 5 years. MASP will band together the Strategic Research Agenda (SRA) of ENIAC with die Annual Work Programme (AWP).

During edaWorkshop09 (which has been organized together with the CATRENE/MEDEA+ DTC) in Dresden, the edacentrum collected the industrial requirements of the next MASP and discussed this input with the workshop participants.

The collected technical requirements will be evaluated and discussed again by annual MASP working groups. All experts further on are invited to send their industrial requirements to the edacentrum to complete the MASP 2010.

Abbildung 4.01: Experts wrote and discussed about the MASP 2010 at the edaWorkshop09

Call for tender on "Design on Future Embedded Systems" has been launched

The call for tender on "Design on Future Embedded Systems" has been launched on 20 June 2009 (identifier 2009/S 117-168440). The FP6 IST & FP7 ICT R&D programmes and the set-up of the ARTEMIS joint technology initiative have created an identity in the European community of Embedded Systems. The objective of the call is a study, which is aimed to