MEDEA+ aims to keep Europe independent in microelectronics

Excellent progress in pan-European precompetitive collaborative work was announced at the annual MEDEA+ forum, held in Berlin in late November. MEDEA+ (MicroElectronics Development for European Applications) is an industryinitiated, eight-year program that terminates in 2008. It follows efforts such as JESSI (Joint European Sub-micron Silicon Initiative, 1989-96), which put Europe's struggling R&D back onto the world map, and a 1996- 2000 MEDEA program aimed more at applications. MEDEA+ aims to make Europe a leader in system innovation on silicon, by providing technology platforms that will allow European companies to maintain their positions as worldwide leaders.

Pre-1990 European work was fragmented by national boundaries that limited investment. MEDEA+ stimulates intensive trans-border cooperation between large, medium, and small electronics companies, their suppliers, system integrators, universities, public laboratories, and research institutes. Every MEDEA+ project has brought together academic and industrial partners from at least two countries. There are now over 280 partners from 16 countries in 56 projects involving resources of 13,650 person- years at a cost of about $500 million/ year. Henryk Fiedorowicz, director of the Institute of Optoelectronics, Warsaw, Poland, told *WaferNews* that his institute is the first partner from Eastern Europe to be accepted by MEDEA+ for a project on laser plasma extreme UV (EUV) sources using a xenon gas target. Arthur van der Poel, the new chairman of MEDEA+, said, "The overwhelming response by MEDEA+ partners clearly has demonstrated the continuing commitment of Europe's microelectronics industry to invest in innovations and R&D." He claimed the European industry continues to lead the world at converting its R&D investments into successful commercial products. "We took the deliberate decision to focus on innovations and a strong microelectronics R&D." He stressed that Europe must now build on its success, and that any hesitation to implement its chosen strategy may result in an irreversible closing of the window of opportunity.

Van der Poel showed that public investment in European microelectronics has remained fairly constant at about $140 million annually over the past ten years, while participating companies increased their R&D costs six times in this period, and in the US, federal support rose by nearly three times to more than $2 billion. He said Europe is at the crossroads: If its R&D investment shrinks, R&D and nanoelectronics will move elsewhere with thousands of jobs lost—but with a joint effort from industry and governments, the future of the European nano-technology industry can be secured.

The MEDEA+ technology projects are in line with the International Technology Roadmap for Semiconductors (ITRS), which maps required technology development, including gaps, barriers, and bottlenecks to be solved. MEDEA+ has set up an Applications Technology Roadmap (ATRM) that reverses the process by starting with the envisaged future needs of end users. It is believed

that this roadmap presents a new approach toward better prioritization of investments in technology development for microelectronics applications. This ATRM will try to identify enabling applications and technologies that must be mastered on time to satisfy user needs in 2012 identified as part of this roadmapping activity. The technologies to be adopted should be far enough developed for use in mass production in 2012, and will be the basis for future R&D in MEDEA+, its successors, and other programs. The scope of the ATRM is determined by applications that originated from collected end-user needs, and some are already in the MEDEA+ program: fixed and mobile communications, automotive electronics, smart cards, multimedia and Internet consumer capabilities, etc. Others such as health, education, and comfort are not currently covered by MEDEA+.

MEDEA+ supports two project domains: applications and technologies. The applications domain includes high-speed communications and system-on-chip design, with an average project size of some 250 personyears. In the technology domain, the greatest future challenges are in the EUV lithography and sub-100nm CMOS technologies. The four EUV lithography projects cover sources, masks, the preparation of an alpha tool, and imaging technology, for a total of over 1700 person-years, but many EUV lithography research problems remain to be solved. Core and dedicated CMOS process development includes seven projects with 2600 person-years.

A notable success has been a pilot line 90nm core CMOS process using 193nm lithography with refined phase-shift masks and optical proximity correction. This T201 process achieved physical gate lengths of less than 65nm. Normal oxynitride dielectrics are used, not high-k ones such as HfO2 that were investigated. As one of the most advanced processes in the world, it will be used to produce 90nm devices on 300mm wafers. All achievements are benchmarked to stay in line with the ITRS.

Further details on MEDEA+ can be found at: www.medeaplus.org.

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