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News Article

Europe pushes ahead of ITRS

News:Process development

The European Commission NANOCMOS project began March 1, 2004, to push the semiconductor industry to 45nm production and beyond. The first phase is for 27months up to June 2006. The next phase will need European Commission and MEDEA+ approval and calls for participation are expected to begin in mid-2005 for a start in 2006.

All three of the main European integrated device manufacturers (IDMs) are participating – STMicroelectronics, Philips and Infineon Technologies. ST and Philips also work on 45nm processing with Motorola at Crolles in France. The US company is not yet in NANOCMOS, but is expected to join soon. In Europe, NANOCMOS results will have an impact on the technology choices for 45nm CMOS logic processes at Crolles, France, and the DRAM activities of Infineon in Dresden, Germany.

The first phase aims to demonstrate feasibility of a 45nm process within 24 months – by December 2005 or earlier. At a meeting in Turin (September 11, 2003), project leader Guillermo Bomchil of ST expressed the hope that the second phase would include a MEDEA+ project with first full integration on 300mm wafers in 2007. Further, the phase should include an Information Society Technologies (IST) project to demonstrate feasibility for 32nm CMOS logic in early 2007. Some preparation work for 22nm is also envisaged.

The proposed work programme aims to get results that will achieve industrialisation ahead of the schedule given in the 2003 International Technology Roadmap for Semiconductors (ITRS). The ITRS has 45nm industrialisation scheduled for 2010.

The procedures are similar to previous European collaborations on 90nm and 65nm technologies. These projects fed into MEDEA+ structures in the second phase before transferring into individual commercialisation work by the industry partners. NANOCMOS will make a proposal to MEDEA+ to start in 2006 on the integration and validation of the 45nm node in an industrial 300mm wafer manufacturing facility, currently expected to be the Crolles2 facility jointly shared by Motorola, Philips and STMicroelectronics.

Besides work at IC manufacturing facilities, much of the NANOCMOS work is expected to be carried out at the two main European research centres - IMEC (Belgium) and LETI (France). Other research interests include three of the Fraunhofer Institute labs and eight labs under the CNRS French research body. Philips Research will also contribute from its Leuven (Belgium) and Eindhoven (The Netherlands) operations. One research laboratory from the Technical University of Chemnitz (Germany) is also participating.

Small-medium enterprises (SMEs) are participating – Magwell, a Belgian spin-out from IMEC, Isiltec, a German chemical-mechanical planarisation (CMP) tool provider and IBS, a French supplier of low-energy implant tools. A further SME (ACIES, France) is helping NANOCMOS in management procedures for the project. Additional partners could be incorporated into the consortium in the future.

The main goal of the research is to demonstrate the feasibility of a 45nm process through a static random access memory (SRAM) test chip. There are still many options for the final process and part of the aim of the project is to narrow these down and make some choices. These choices concern factors such as whether to use bulk silicon or some advanced substrate such as silicon-on-insulator (SOI) and/or strained silicon. And it's not just materials that are under review –the move to 45nm might require different transistor architectures such

as silicon-on-nothing (SON), FinFETs or some other structure.

By month 18 of the project, it is hoped that these choices will have been made clearer and that by then the team will be able to choose one or at most two to develop further. EC rules stipulate that it can only supply around 50% of the finance. The first, 27-month phase is budgeted at EUR50mn, with at most EUR24mn coming from the EC. An executive board consisting of representatives from the core group of IDMs and two co-opted members will make decisions on the project. There is also a general assembly in which all partners are represented and decisions made by qualified voting procedures.

There is also management team to make day-to-day decisions for the ten sub-projects. Eight of these cover technical areas, with two more for training and dissemination of information. The eight technical areas will deal with new materials and front end modules, new device architectures, new multilevel metallisation materials and structures, physical and electrical characterisation , simulation and modelling, new concepts for integrated metrology, and integration of a 45nm CMOS process including feasibility demonstration of an SRAM cell.

The EC has also agreed to sponsor a complementary SINANO ‘network of excellence’ to gather together work by European public research laboratories working in the field of novel devices.

Picture: The launch team for NANOCMOS