Cooperation in European microelectronics R&D

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ABSTRACT

A growing gap in microelectronics technology in Europe mainly versus US- and Japanese practise, a rising awareness that leadership in electronics is decisive for progress and wellbeing of industrialized nations, and semiconductor innovations being the key-enabler for almost all technical advances of industry, has led in the middle of the 80´s to the first initiatives of private, public partnership (PPP). For the future, these PPPs will continue demonstrating their effectiveness in securing R&D and advanced manufacturing in Europe, if reciprocal qualitative and quantitative commitments are taken by Industry and European Public Authorities.

Making up time

The programmes launched as part of the EUREKA initiative, JESSI, then MEDEA and MEDEA+, complementing the Framework Programmes of the European Commission, backed up the industrial efforts both politically and financially. These programmes, widely recognised as successful, did more than provide indispensable financial support: they played a key role in the construction of efficient cooperation throughout the value chain, by generating synergies between manufacturers of equipment for semiconductors, hardware producers, semiconductor manufacturers, electronics companies and "design houses".

JESSI (1989-1996) primarily focused on closing the technology gap with the US and Japan, MEDEA (1997 – 2000), thanks to the platform laid by JESSI, has been able to play a more forward-looking role by strengthening R&D cooperation of System suppliers and Semiconductor companies. MEDEA+ (2001 – 2008) will help Europe to become a leader in System Innovation on Silicon with a strong leverage effect on industry, economy and the society at large. The programmes enabled the European semiconductor companies to take an early leadership in strategically chosen core competences: multimedia, communications, automobile and traffic applications, design techniques and libraries, CMOS based technology platforms and equipment and manufacturing technologies.

Europe now has three semiconductor companies in the world top ten: STMicroelectronics, Infineon Technologies and Philips Semiconductors.

The success of Europe's chip industry has also brought success to its partners, customers and suppliers: Customers such as Alcatel, Bosch (being not only a leading supplier to the automotive industry but also climbing up as number 2 semiconductor supplier for the automotive market in Europe), Bull, Ericsson, Nokia, Philips Consumer Electronics, Siemens and Thomson multimedia, and many SMEs as well, have benefited by increased competitiveness. European systems companies now lead the world in GSM telephony and access networks, smart cards, automotive electronics and digital consumer products.

Suppliers such as Air Liquide, ASML, ASMI, Carl Zeiss, Leica, M+W Zander, Jenoptik, Recif, Schlumberger, Soitec, Wacker and many others have benefited by strengthening their position as suppliers to semiconductor companies across the globe. Research institutes and universities have also participated directly in the growth of the European microelectronics industry.

All this has been achieved through a greatly increased willingness to cooperate. Indeed JESSI, MEDEA and MEDEA+ are the leading model for trans-national, cooperative, pre-competitive research in the world, demonstrating how cooperation cuts development time, risk and cost.

Entering new financial challenges

As for all large market areas electronics and microelectronics become increasingly 'global'. This is true of course for the market since production in volume at favourable economic conditions means standardisation of the products. But this is also true for manufacturing and even for R&D. However with each one new generation of process equipment, the investment necessary is extremely going up.

Manufacturing: if a state-of-the-art manufacturing line for 200 mm diameter wafers priced about $ 1 to 1.5 B, for the same output in wafer counts it costs $ 2.5 to 4 B for 300 mm wafers. Of course, this unit will deliver about twice the number of chips that the first one was able to manufacture, but the initial cash out investment necessary to have it starting will discourage many investors, even world wide players.

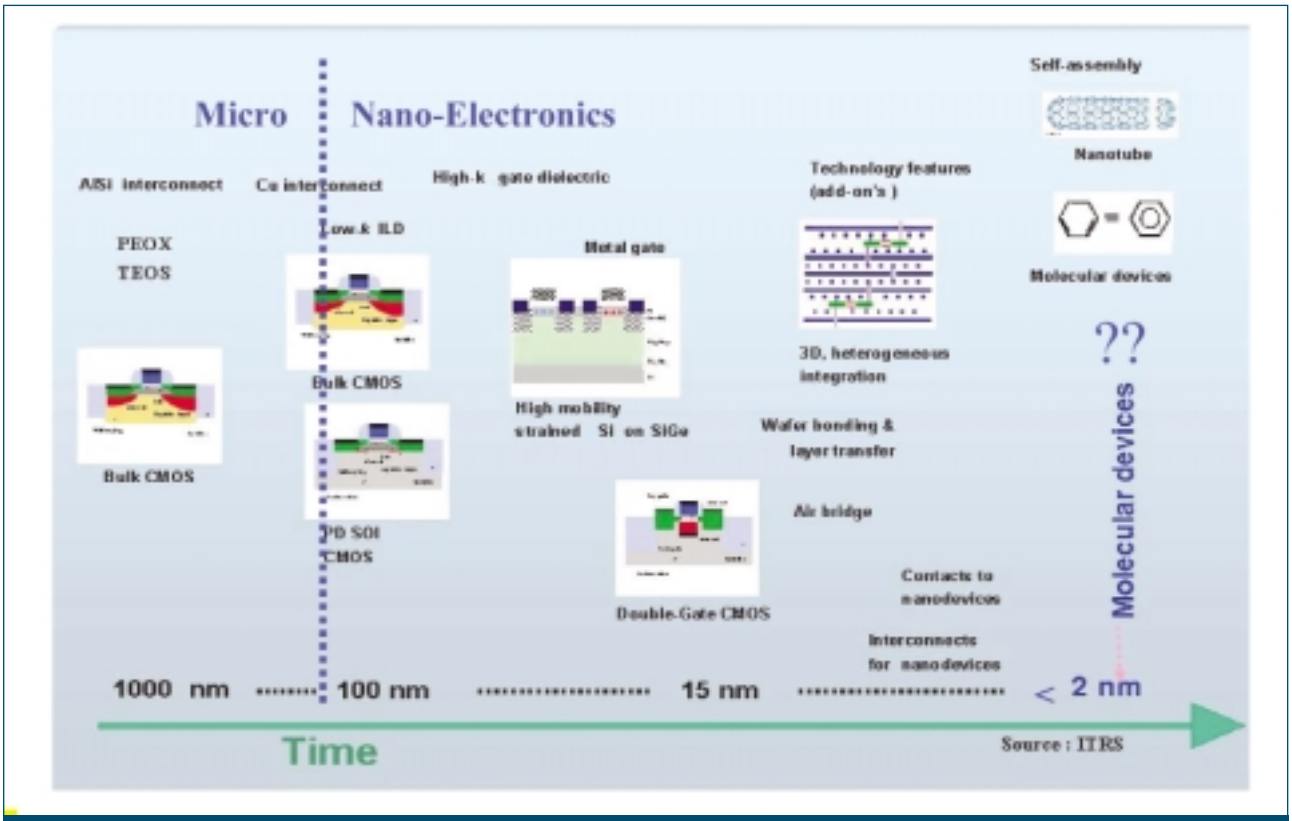
Research and development: similarly, the cost of R&D increases with complexity making it difficult for second tiers and even specialised players to follow the ITRS pace. The latest evaluation for the 90 nm process development cost exceeds 1.5 B$! Not many companies can afford such a huge investment, just for the mastering of the enabling technology.

The cost of mask sets follow an exponential law quite similar to the reduction of feature sizes. For the 120 nm process generation, a mask set is priced in the range 350-500 k$; when now entering into production 90 nm generation it will reach 1 M$ and the previsions for the 65 or 45 nm next generations are even more threatening. Since, due to the increasing design complexity, nobody can guarantee before starting the silicon processing that the design is 100% defect-free, financial risks are skyrocketing.

From micro- to nanoelectronics

Microelectronics is the only currently available technology where the costs per function are regularly decreasing while the functionality is steadily increasing. This allows market's expansion and the dissemination of economic progress, which is the engine for growth. For the next 20 years, there are no other viable technological alternatives to put together millions of tiny structures with close to 100% manufacturing yields.

This by no means implies that the semiconductor industry will not rejuvenate itself. In addition to the well known scaling effect (the 'Moore's



A continuous move from the micro to the nano world

law'), continuous progress will be made possible by the use of complementary materials and innovative techniques when stepping down to 'nano-technologies'.

Already now, leading edge semiconductor manufacturing processes involve sub-100 nm drawn lines and sub-10 nm layer thickness within mastered recipes and with monitored yields. Nanotechnologies are already a reality in the microelectronics domain where they are extensively used in volume manufacturing. Looking forward into the future, experimental silicon structures down to 7 nm, well into the 'nanoelectronics' world have been already demonstrated (see Chart 1.) Before looking to other 'exotic' alternatives the full potential of nanoelectronics on silicon will have to be explored and the introduction of new features coming from the 'nano' world has to be seen as a logical and necessary step in the microelectronics technology evolution. Up to 2020, or beyond, silicon-based technology will remain the dominant force.

The new ITRS (released in December 2003) forecast no new acceleration. The rhythm of 'technology nodes' replacement remains unchanged vis-a-vis the 2001 release: 3-year cycles will prevail. Next nodes may start ramping-up in production in 2010 (45nm), 2013 (32nm), 2016 (22nm) and 2019 (16nm).

These goals and all the intermediate steps will however only be reached if the numerous 'road blocks' on the increasingly bumpy silicon highway find on time and economically viable solutions.

Increasing complexity, decreasing time-to-market

The mastering of complexity is the next major challenge for the semiconductor industry in the next 5-10 years. While the new processes allow to integrate increasingly more transistors on one single chip, designers are confronted with increasing complexity and have to face a growing design-process gap making difficult the full exploitation of these technologies on-time.

Challenging system requirements such as higher operation frequencies, lower power dissipation and increasing reliability demands, e.g. in the automotive or smart-cards markets have to be answered properly, also having in mind shorter time-to-market and time-to-volume. This is a major issue for both system and devices manufacturers.

The shortening of the design cycle, combined with the increasing complexity of the chips to be manufactured naturally calls for closer relationship between the system manufacturers and their IC suppliers to validate their specifications in the early stages, not waiting for long and expensive silicon-proof. The complexity will also force the semiconductor manufacturers themselves to imprecate more closely design and process development. Predictive EDA and Technology CAD (TCAD) are 2 strategic enablers of this new approach.

The manufacturability and the repairability of the chips themselves will also have to be anticipated from the beginning of the design process: fault observability, process/device optimisation, design for repair are promising techniques to cope with the growing cost of manufacturing linked to the growing complexity. We just entered the 'design for manufacturability' era: the main target is to increase the number of Good Dies per Wafer.

Increasing need for private public partnership

Europe's independence and economic future will largely depend on its ability to cope with the permanently renewed challenges posed by both the market demand and by its main geographic competitors.

Above, reference has been made to changes and challenges mainly as a

result of technical innovation. There is one more threatening scenario for Europe. Induced by increasing industrial globalisation, a worldwide regional race for leadership in microelectronics has started. Governments are attracting high-tech companies by offering an extensive funding policy, motivating investors with preferential "operational conditions", i.e. fiscal privileges, tax exemptions, grants, loans, subsidies etc.

Clear examples of the strategic role microelectronics plays in the country's economy have been already given in the past by Korea. More recently Taiwan experienced the same successful growth, becoming a world micro-electronics power. In Japan, over 1B$ of public money is injected per year in support to co-operative R&D and infrastructure. The next new 'big player' is China with the same political wish to encourage local and foreign investment through attractive funding schemes. Shanghai and Beijing are already at fight to offer the best conditions to set up 300 mm silicon factories. In the US, funding support to the ICT industry in general grew from about $ 1B in 1997 to $ 1.9 B in 2002 and will continue growing. For the microelectronics sector stricto sensu, the federal support to academic and industrial R&D is now in excess of 1.3 B$ per year. More recently the States also entered into the loop with for instance a support from the State of New York to the University of Albany and International Sematech North of 600 M$.

Conclusion

European industry is by no means able to compete with these regions if it does not receive the same support. Today, all public (local, national and EC) means combined lead to a support in R&D infrastructure and activities worth about 600 million euro/year in Europe. There is definitely a strong need for increasing it to put the European players on par with their main competitors. The initiative of private public partnership has to be readjusted in a way, that Industry and Public Authorities are qualifying and quantifying reciprocal commitments, in particular in high-tech activities like nanoelectronics R&D.

If Europe is to become "the most dynamic knowledge-based economy in the world by 2010" as stated in 2000 by the Lisbon European Council a stimulus for growth, employment and innovation is urgently needed.

ENQUIRIES

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