Advanced engineered substrates boost chip performance

Technology / Semiconductors

A single platform that combines the benefits of strained silicon and silicon-on-insulator technologies hopes to offer much improved performance for future chip generations. The EUREKA MEDEA+ Cluster SilOnIS project developed new substrate materials for producing high-speed, low-power integrated circuits. SilOnIS built on the strengths of the main European players in substrates, chipmaking and metrology to combine high-mobility wafer-level strained silicon and so-called silicon-on-insulator (SOI) technology in a single processing platform to provide high-performance chips. SOI architectures offer higher speeds and lower power consumption than bulk silicon, while strained silicon improves performance further. Suitable wafers have been demonstrated targeting device fabrication at the 45-nm half-pitch node and below, in line with global industry needs.

Identity validation, security and privacy are critical issues around the globe. Smartcards containing a Silicon wafers or substrates are the key to modern electronics components. However, as electronics chips become ever smaller, conventional plain silicon is no longer capable of providing the necessary performance. This has led to techniques such as applying a strain field to the semiconductor active layer to boost the speed at which an electronic signal may be transferred. However, the smaller the device, the more difficult it is to apply such a strain.

A fast-developing addition is SOI technology. This involves applying an ultra-thin silicon film to the silicon wafer to provide an intermediate insulation layer. Chipmakers can fabricate their integrated circuits (ICs) on the top layer of SOI wafers using the same processes they would apply to plain silicon. The wafers are then cut up as normal and the chips packaged and integrated into electronic systems such as personal computers (PCs), game consoles, mobile phones and other communications devices, personal digital assistants (PDAs), consumer electronics and multimedia equipment.

SOI offers semiconductor manufacturers two important advantages: it considerably increases the speed of the electronic circuitry by enhancing charge carrier mobility further, while reducing power consumption three or four times. As a result, this technology is being adopted rapidly by major chipmakers to meet the demands identified by the International Technology Roadmap for Semiconductors (ITRS).

The MEDEA+ SilOnIS project set out to combine the advantages of both the strained layer and SOI technologies in a single strained SOI substrate technology platform. It brought together the different elements of the microelectronics chain: substrate and materials suppliers, chipmakers and metrology equipment manufacturers.

European substrate suppliers have been able to reinforce their leading position in the high added value segment of engineered substrates while counterbalancing Japanese leadership in bulk silicon. Chipmakers have gained early access to innovative solutions that will strengthen Europe's position in low-power and high-performance components. And several complementary metrology and characterisation equipment suppliers have been able to develop specific metrology or specific ways of using standard metrology for this key area.

This MEDEA+ project is only the first step in the engineering of advanced substrates for integrated circuit production. Europe has a strong position in this field with SOITEC as a leading actor and Siltronic actively entering the area.

'The idea of the project emerged in different places in the minds of several actors involved on one hand in advanced substrates and on the other in integrated circuits,' says Bruno Ghyselen of substrate supplier SOITEC, which helped initiate the project and acted as project leader. 'Close collaboration between substrate manufacturers and chipmakers was essential to match the developments in the two complementary fields.'

'Carrying out such a collaborative project in the framework of EUREKA brought additional benefits,' he adds. 'Sharing the risks and the financing was a real enabler to undertake

» Next Article in Technology - Semiconductors: **Breaking the performance barrier of 22-nm CMOS technology**