CMP United Business Media
EETIMES ONLINE europe
Global news for the creators of technology

Borel's European chip industry proposal in full

Joseph Borel, JB-R&D
(03/18/2008 10:14 AM EDT)
URL: http://eetimes.eu/germany/206904289

Joseph Borel, former executive vice president in central research and development at STMicroelectronics NV, has sent a 12-page proposal to the French government calling for the consolidation of Infineon Technologies, NXP and ST into a European champion chip company. *EETimes Europe* obtained a copy of the proposal, entitled: "Nanotechnologies in Europe: There is room for a single profitable share application-driven foundry". Borel gave *EE Times Europe* the authorization to publish it.

Foreword:

Joseph Borel, former executive vice president in central research and development at STMicroelectronics NV, has sent a 12-page proposal to the French government calling for the consolidation of Infineon Technologies, NXP and ST into a European champion chip company.

EETimes Europe obtained a copy of the proposal, entitled: "Nanotechnologies in Europe: There is room for a single profitable share application-driven foundry".

Borel has given *EE Times Europe* the authorization to publish it. Here is the full text.

Nanotechnologies in Europe: There is room for a single profitable shared Application Driven foundry!

1-European critical situation

Looking at European semiconductor business versus worldwide competition brings some concerns about what is going to be the short term perspective of technology development for several reasons:

-Recent decisions show a willingness for semiconductor companies to disinvest in terms of foundry business, expecting their semiconductor chips to be made by foundries.

-European semiconductor companies on the other side have strong expertise in mixed analog digital, an added value for most of the new applications on the market (wireless, automotive…).

-This is well suited for the needs of European system houses very competitive in several markets such as wireless, automotive, consumer…

-The size of the European semiconductor companies is too low for facing individually the huge investment constraints in their separate fabs.

-Nanotechnologies to some extend are close to full custom though handling huge amounts of digital devices complexity (several hundred thousand devices per chip including analog and digital blocks).

-Design costs are so high that only a few, large volume, application sectors will allow a return of investment.

In this context the R&D activity is generally of high quality and the "international poles of competencies" can efficiently help in the industry support.

When looking at the top 25 in the market share ranking, the three European semiconductor companies total a worldwide semiconductor revenue of $26.484 billion, still below the $31.289 billion performance of Intel alone (first of the list even if declining 9.5 percent in revenue versus 2005).

2-Cost of nanotechnologies

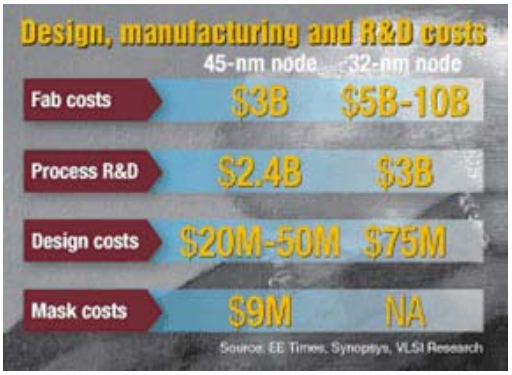
-It is known that process R&D, design and manufacturing costs are skyrocketing when moving to 45-nm node and below.

-This means that only a few organizations worldwide will be able to support such costs that should be driven by a significant worldwide market share.

-Consequently, there is a mandatory need of synergetic cooperation move underlying this statement among the semiconductor companies to survive.

-Pure foundry business is likely to be limited to purely digital products in the short term.

-Following the cost factors given in the following figure, an amount of $5.4 billion is necessary as an entry ticket to enter the 45-nm game (Fab and Process R&D costs).



Source: EETimes 03/30/2007

-then there is a need of a strong design team to address the new challenges of designing hundred million gates, with careful handling of low power consumption, manufacturability including variability contribution and dependability (versus process, soft errors, EMC…).Costs of designing are estimated to run between $20 to $50 million.

-mask costs for a single product are evaluated at $9 million.

3-Interdependence between product and process

Taking as an example the Intel dual core 64b Merom processor (ISSCC 2007 paper 5.6), the main chip applications covers several domains of the server/desktop/mobile markets:

 *See related image*

This is typical of a large and wide application market with very advanced features for the corresponding chips to comply with the constraints of the application through a tuning of the silicon process.

Behind such a design there is a tremendous work of technology R&D to study in detail all the technology features/corners for getting the best tradeoffs between performances and manufacturability for these specific product ranges (mostly mixed analog and digital design), the root to increased market share and sales margins.

Design peculiarities of Merom are:

-complexity: 291 M transistors in 65-nm process and copper interconnect layers on a 1.43 cm^2 chip

-0.85 volt min operating voltage in some areas (PMOS devices as sleep transistors for operation at 500mv below chip Vcc)

-sleep and shut off modes

-Fault tolerant cache

-Techniques for speed debug and test

-Thermal management SW through analog and digital thermal sensors

-8 copper interconnect layers and low-K carbon doped oxide inter level dielectric (k=2.9)

These figures show how important is the link between "market-product-technology features-manufacturability."

Obviously this strategy needs a good connection with applied research centers in process, characterization, device physics,

components physical characterization, analog design and a deep understanding of the end product market evolution (new applications and new advanced products capabilities).

4-Dedicated silicon foundry threat

Capital investment figures of several B$ are a strong limitation in the proliferation of "dedicated products" semiconductor plants, and the logic of foundries (called dedicated silicon foundries) lies behind this simple concept. They allow an optimum economic balance (return of investment) provided that they have a single (or limited number) of running processes (mostly digital) in large manufacturing plants fully loaded by numerous customers with rather well defined product categories to manufacture.


See related image

Figure 1: Total IC and foundry revenues
Figure2: A/B: IC foundry revenue/related IC revenue

The above *figure 1* gives the comparison of total foundry market versus total IC market showing the increased contribution of a dedicated foundry (TSMC) to the dedicated foundry market growth.

Figure 2 gives foundry revenue relative to total IC revenue (A) for foundries and (B) for finished products revenues from wafers coming from foundry wafers.

An estimated ratio of 2.5 is given between finished product revenue from wafer foundry silicon (foundry business) versus foundry wafers revenue generating these products (IDM business).

This clearly shows a potential upside for foundry revenue of 2.5X if they decide to move to product design and capture the whole semiconductor market, performing product design and library design in low cost countries associated with significant margins.

Another interesting trend of foundries forecasted business evolution is described below (*figure 3*). Most of their business is today done in logic where they can be competitive without too much investment in advanced critical process steps.

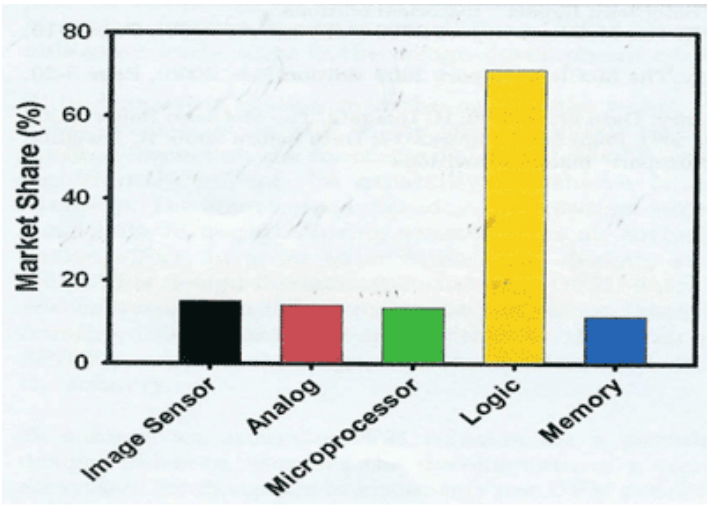


Figure 3: Foundry share of major IC market segments.

They also clearly state their willingness to develop their business in higher value processes (analog, image sensors, microprocessors…) with higher margins, a path to access the overall semiconductor market.

This trend is already depicted in their present technology offering (see the case of TSMC in green on *figure 4*).


See related image

Figure 4: TSMC technology offering (in green) beyond their present digital business

5: The Intel way

As mentioned earlier Intel has been designing complex mixed A-D systems on a chip with in mind a complete process of coming from (huge) markets like multi application processors (servers, desktop, mobile processors) associated with a nice optimization of elementary devices to achieve the best tradeoff in terms of performances (power consumption versus speed, versus functionality-analog or digital devices).

This way, very complex products can be built for large markets, matching by construction the constraints of the end market and giving added business margins versus less sophisticated integrated solutions.

The Merom processor is an early example of what a process-device & design optimized chip can bring in terms of overall

performances (digital, analog, very low power, error correction, disable non used functions, thermal control, speed debug and test functions…).

The 65-nm technology itself uses several supply voltages (0.85 to 1.325 volt) on its 143 mm^2 and 291 Mtransistors.

 See related image

Figure 5: Die photograph of the Merom chip from INTEL

Thanks to developments in all the steps of the value chain, from process and device physics to circuit and architecture smart behavior added value can be brought in products to be manufactured internally by the company, with little possible competition in terms of performance and cost.

This strategy explains why Intel has led and continues to lead the semiconductor business as seen below.

 See related image

The results of this strategy are quite obvious on the above table.

There are two simple equations in terms of sales:

-INTEL sales equal (Samsung+TI) sales (1=2+3).

-or INTEL sales equal (STM+Infineon+NXP Semiconductors+$4,804 million).

There is room in Europe for another single "INTEL like" company that corresponds to the consolidation of the existing players with some boundary conditions:

-close connections to System Houses (Nokia, Bosch…); thanks to the past MEDEA+ investments this is already the case but needs to be increased in terms of business.

-more formalized links with European large research centers (LETI, IMEC, Fraunhofer...) to better support architectures, design/ design solutions and process optimization versus applications.

-sharing of process, library, design solutions developments.

-complete sharing of production facilities addressing the detailed technology needs of European applications as a priority.

6: Implications in terms of costs

The cost implications (investment, R&D and product development) must be clearly understood before making a strategic decision because we are dealing with very complex products needing large design teams, additional process developments and appropriate manufacturing facilities.

6.1: Gate count evolution As seen above the Merom Intel processor is a good example of a typical advanced full custom design in 65-nm process.

It is to be understood as a new wave of products to be considered as “system on a chip” with mixed analog and digital capabilities that will be followed by “system in a package” as long as progress will be made in integration of MEMs (Micro Electro Mechanical systems) and NEMS (Nano Electro Mechanical systems) into the same package or potentially on the same chip.

The *figure 6* below gives the gate count achievable for the various technology nodes from 0.18µm to 65-nm for two die sizes as an example (Merom is already more complex than these average numbers).

 See related image

Figure 6: Transistor logic gate count trends versus technology nodes for two typical die sizes of 1 cm^2 and 2.25 cm^2.

6.2: Design costs for typical CMOS logic design

Figure 7 shows the cost evolution of designing CMOS logic products on more and more complex chips with the 90-nm and 65-nm nodes (as a rule of thumb a doubling at every node).Cost figures will even be higher considering mixed analog, digital or MEMs components at different power supplies and including redundancy or ECC (Error Code Correction) or dependability in safety critical applications.

Power control and management will become a common feature in the future systems on a chip.

Very low power consumption will create more vulnerability in terms of Electromagnetic coupling, signal integrity and susceptibility to SEUs (Single Event Upsets) due to natural radiations effects on logic.

 See related image

Figure 7: Design costs for typical CMOS SoC logic chip in various nanotechnologies.

6.3:R&D costs versus technology nodes in nanotechnologies

R&D is becoming a huge and costly task in the coming technology nodes including:

-Clean rooms of ultimate quality in 45-nm and fabrication plants costs ramping up to several $B.

-Process R&D for the new complex doping and lithography equipments with in mind "variability monitoring."

-Design cost including corporate design solutions, mixed analog and digital library offerings (versus product category).

-Highly performing test equipments (analog and digital capabilities) for fast debug of early products.

 See related image

Figure 8: Relative (to CMOS 0.25µm) R&D costs for developing the nanotechnology nodes processes.

6.4: Cost of manufacturing facilities for advanced CMOS processes Manufacturing facilities costs are increasing at a 50-percent rate at each step as seen in *figure 9*.

 See related image

Figure 9: Manufacturing facilities costs in nanotechnologies.

7-Gobal European rationale

The coming evidence is the one of a fierce international competition on the semiconductor market, associated with the need to fuel system development projects in areas where Europe has a leading knowledge:

-telecommunications with NOKIA, Ericson, Alcatel… -Military and avionics with EADS, AIRBUS… -Very high speed trains. -Medical assistance…

All these strategic markets will need a significant amount of advanced SoCs and SiPs available only through a concentration of skills in Europe (strong coordination of national labs in an R&D European FEDERATION sharing scientific programs in equipments, technology, EDA and Design) and common industrial investments in fabs, Technology equipments, processes, IP libraries and Design Solutions to be shared in a single Virtual Organization aiming at the same goal.

-Market rationale: enhancing European system competitiveness in advanced systems and then open to outside market for business in non critical European sectors.

-Production facilities rationale: more outputs in terms of chips with less numerous but more dedicated facilities and serving European needs.

-R&D centers rationale : strongly coordinated and shared processes, equipments, devices, embedded SW , design and design automation solutions development for mastering “variability”, a challenge coming from the more and more atomic size of the devices (need for statistical simulations e.g. as seen below because of the atomic structure of nanodevices).

 See related image

 See related image

In terms of business, here below are shown the Top 10 semiconductor vendors with their market performances in 2006.

 See related image

It is seen that the 3 European semiconductor vendors total some $26,484 billion, representing 84.6 percent of the Intel alone performance.

This shows how is urgent synergetic move of Europe through cooperation and complementary product lines offering through a single European production foundry. There is room for investment rationalization and product synergies between the three European independent players addressing presently some overlapping parts of the market, with no formal agreements on strategic sectors like memories where manufacturing costs are very critical to survive.

The quality of R&D in Europe in large R&D centers, if properly funded and driven by Applications, can help reaching this challenge.

An order of magnitude of the corresponding costs of such a program in terms of facilities and process development, design

costs and mask costs per major product in 45-nm process are summarized below.

 *See related image*

 *See related image*

15 04 2007 **References:**

ISSCC 2007: - Joel Hartmann, "Toward a New Nanoelectronic Cosmology", ISSCC Technical Digests, Paper 1.3, February 2007. -Morris Chang "Foundry Future: Challenge in the 21st Century, ISSCC Technical Digests, paper1.1, February 2007. -Nabeel Sakran, Marcelo Uffe, Moty Mehelel, Jack Dowweck, Ernest Knoll, Avi Kovacks,"The implementation of the 65nm Dual-Core 64b Merom Processor," ISSCC Technical Digests, Paper 5.6, February 2007.

Gartner Dataquest: December, 06 2006.