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EMC concerns all designers here

Richard Goering
EE Times
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Chip, package and pc-board design are typically disjointed domains with their own concerns, design tools and methodologies. But one issue that cuts across all three--and demands greater cooperation--is electromagnetic compatibility.

The Medea+DAC workshop in Germany underscored the need for a better electromagnetic compatibility methodology. Thomas Steinecke, EMC project leader at Infineon, noted that while EMC defines the ability of an electronic component to function reliably under all specified electromagnetic conditions, electromagnetic reliability (EMR) defines the ability of the entire system to function reliably. And EMR is defined by the EMC of all the system components. The key word is "all."

Steinecke noted that more transistors per chip, increasing clock rates and faster I/Os add up to increased emissions. Meanwhile, decreasing core voltages and smaller feature sizes add up to lower immunity.

IC design, said Steinecke, must be "first time right" regarding EMC, with a good EMC prediction during the design phase. Design- and layout-based chip and package models are needed for IC design optimization and EMC signoff. Pc-board designers, he noted, need IC placement and decoupling guidelines from chip designers, plus simple but accurate IC models for system EMC simulation.

IC and pc-board EMC design today, Steinecke said, is based on 50 percent experience and 50 percent black magic. The time is now for a "nonblack magic" solution, he said.

At automotive supplier Bosch GmbH, the European-funded Mesdie project has helped establish an EMC design methodology, said Harald Weller, Mesdie project leader at Bosch. Aimed mainly at pc-board design, the methodology provides automatic checking for some 350 design rules compiled from EMC experts.

To solve the EMC problem, people must leave their cubicles and work with other design groups to understand how their part of the design will affect the entire system.

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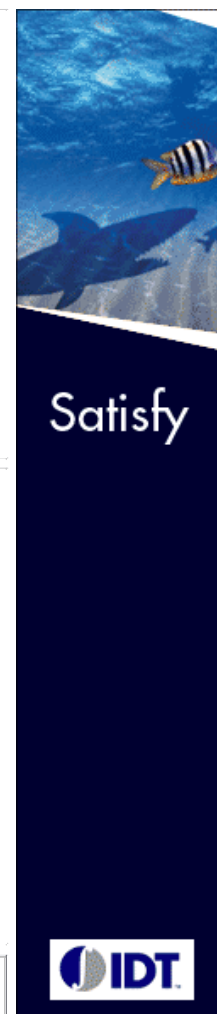
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