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In Europe, EDA bids for respect

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Prien, Germany -- With an eye on tomorrow's systems-on-chip--containing perhaps millions of gates, complex embedded software and integrated nanoelectronics--European systems houses and research institutes are developing next-generation EDA tools and design methodologies. A workshop last week in this Bavarian Alps resort town provided a glimpse of the challenges they face and the successes they've already achieved.

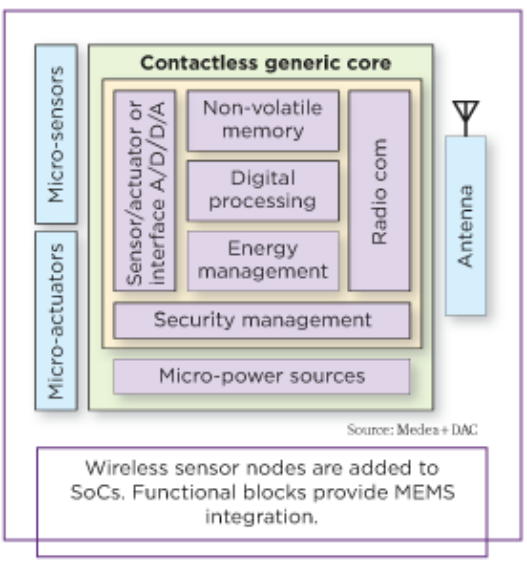
Speakers at the Medea+Design Automation Conference outlined problems and solutions in such areas as electronic system-level design, design-for-manufacturability (DFM), electromagnetic compatibility, nanotechnology integration and analog/mixed-signal design.

Medea+DAC is sponsored by Medea Plus, a government-financed consortium seeing to bolster Europe's microelectronics industry. Several Medea-backed projects were described at the conference, including one that helped launch an analog design tool startup.

"People ask why the main players in EDA are all U.S.-based," said Andreas Ripp, vice president of sales and marketing for startup MunEDA (Munich, Germany). Anastasia, a Medea Plus project researching analog enhancements for a system-to-silicon automated design, led to MunEDA's analog optimization and DFM tools. The project shows that "successful EDA innovation can also start in Europe," Ripp said.

Far more than conventional digital design is at stake, speakers noted. Mart Graef, strategic program manager at Philips Semiconductors, showed a Nokia SoC in which 75 percent of the cost is nondigital. He also described a "more than Moore" trend toward systems-on-chip with integrated analog/RF components, sensors and actuators, radios, and fluidics.

Some at Medea+DAC discussed the two hottest areas for EDA innovation, electronic system level design (ESL) and DFM. There's a relationship between them, said Artur Weller, senior principal for design methodology at Infineon Technologies. "The designer who goes to a higher abstraction level easily loses sight of what's behind the technology," he said. "There's a good chance that we'll move the abstraction level to TLM [transaction-level modeling], but we must also keep track of design-for-cost and -manufacturing."



One of the most successful EDA-related initiatives with European roots is Spirit, which defines an XML schema for

intellectual-property configuration data. Ralph von Vignau, director of platform infrastructure at Philips Semiconductors and chairman of the Spirit Consortium, told Medea+DAC that Spirit is seeking standardization as IEEE P1685.

Cutting-edge research

At the Leti research institute (Grenoble, France), a design flow using functional blocks of wireless sensors for actuation, wireless connectivity, embedded intelligence and energy management promises to bring microelectromechanical systems into SoCs, said Hughes Metras, who heads Leti's smart-devices program. The sensors have both analog and digital elements.

France finances much of the work, which began two years ago with ultralow-power radios. The flow encompasses detailed system models, MEMS physics and extraction-based models, electrical models of MEMS functions and automatic synthesis of RF functions. It supports co-design of MEMS and electronic functions. Tools include Matlab, VHDL-AMS simulation, RTL simulation and transistor-level simulation.

Medea's Anastasia project culminated in a commercial design tool delivery, said MunEDA's Ripp. The project ran from 2001 to 2005, encompassing IDMs, systems houses, EDA vendors, universities and research institutes. It sought to speed synthesis of analog system components and to facilitate process migration and reuse of analog blocks.

The resulting product, Wicked, is a tool suite for analog/mixed-signal analysis, optimization and DFM. It's sold in the States by ChipMD Inc., an independent company largely owned by MunEDA.

Another analog/mixed-signal project, SpeAC, focuses on system-level design. Participants include European system houses and IDMs, along with EDA providers Synopsys and Cadence.

Patrick Birrer, an applications engineer at Cadence Design Systems GmBH (Feldkirchen, Germany), described three project accomplishments, including linking SystemC into the analog/mixed-signal environment, automatic VHDL code generation from The MathWorks' Simulink product, and co-simulation between Simulink and Cadence's AMS Designer suite. Bosch has integrated the Simulink VHDL capability into its design flow. The AMS Designer link "will be included in the next Cadence product release," Birrer said.

At Infineon, CAD researchers are integrating statistical timing analysis into the design flow, said Harald Kinzelbach, senior staff engineer for statistical modeling. Process variations become random variables that can have a profound impact on chip timing, even changing an "uncritical" path to a critical one, he said.

Statistical timing analysis can account for random variations by propagating delay distributions through a circuit, but Kinzelbach sees problems. Since global variations and topology cause correlations everywhere in the circuit, he argued, "local probability distributions are of no use at all" as a primary input for statistical analysis. The better approach, he said, is to use cell response as the first input and calculate final distributions later.

EMC and ESD

Thomas Steinecke, who leads the electromagnetic compatibility project at Infineon, described efforts to bring "electromagnetic reliability" to ICs and pc boards. EMC is a key criterion for automotive applications, Steinecke said, with chips generating emissions through intended and unintended switching. ICs also exhibit increased emissions because of growing transistor counts, clock rates and I/Os.

Calling the handling of EMC "50 percent experience and 50 percent black magic," Steinecke said Infineon is working to replace some of the magic with modeling. What's needed, he said, are EMC models along the design chain for chips, packages and boards. European-funded projects are aiding in that quest, including the Mesdie modeling initiative and its successor, Parachute.

Harald Weller, Mesdie project leader at Bosch GmbH, said that since EMC has too many requirements for manual control, they must be checked automatically during development. After collecting more than 350 EMC design rules from its EMC experts, Bosch is bringing them into a design flow in which the rules can be checked automatically, he said.

Another design concern that's had little EDA support is electrostatic discharge. Wolfgang Stadler, principal for ESD verification methodology at Infineon, de- scribed his work with a Medea Plus project looking at application-specific design that addresses ESD and substrate effects.

Companies participating in the project are developing a charged-device-model test strategy, including test structures, a package emulator, characterization and circuit simulations.