NANOCMOS Project to Explore Limits of CMOS

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Europe is big on large, collaborative research projects, and why not? There's readily available government funding, dozens of world-class research institutes and several key consortiums, several big IC manufacturers, and the world's third largest concentration of equipment and materials suppliers. The latest and perhaps most ambitious project to date is called NANOCMOS, which aims to "pioneer the necessary changes in materials, processes, device architectures, and interconnections to keep pushing the limits of semiconductor performance and density." NANOCMOS is designed to integrate the CMOS activities that in the past have been the object of ES-PRIT/IST and JESSI/MEDEA.

Participants in the project will be charged with demonstrating the feasibility of 45 nm CMOS logic technology in 2005, while simultaneously starting research activities for the next-generation 32 and 22 nm technology nodes. Today, these smaller nodes are considered at the limits of present technologies, and may require the use of new nanotechnologies, such as silicon nanowires and carbon nanotubes.

The key objectives of the NANOCMOS project are to:

- Integrate in a coherent structure all the European R&D projects and different sources of financial support and instruments, in the domain of NANOCMOS technologies, to help the European microelectronics industry to keep its place among the few worldwide leaders in the field.
- Make a substantial contribution to optimize efforts in microelectronics, coordinate the efforts in microelectronics between FP6 and MEDEA+, reinforce collaboration between industrialists and academic research centers, and overall strongly contribute to structure the ERA in microelectronics.
- Implement a large, cooperative R&D project enabling the introduction of the necessary changes in the materials, process modules, device architectures, multilevel metallization structures and all related characterization, test modeling and simulation technologies to keep the scaling trends viable and make all future IST applications possible.
- Start at the right time a project that proposes the highly ambitious objectives to achieve a demonstration of feasibility of a 45 nm CMOS logic as early as 2005, a first full CMOS process integration in 2007, and a demonstration of feasibility of a 32 nm CMOS logic process as early as 2007.

The partners in the project are Europe's three largest semiconductor companies — Infineon, Philips and STMicroelectronics; the two largest European technological research institutes — CEA Leti (France) and IMEC (Belgium); three research laboratories coordinated by the Fraunhofer Gesellschaft (FhG, Germany); eight research laboratories coordinated by the CNRS (France); one research laboratory from the Technical University of Chemnitz (Germany); three other companies — Ion Beam Services (France), ISILTEC (Germany) and Magwel (Belgium); and ACIES Europe (France), which will undertake some management aspects of the project. Additional partners could be incorporated into the consortium in the future.

"Because of its ambitious objectives and committed resources that are mobilized for a common goal, NANOCMOS represents a unique opportunity for Europe to become the leading center for nanoelectronics, while supporting academic research and helping its indigenous industrial players to hone their competitive edge," said Guillermo Bomchil, leader of the NANOCMOS project, in a statement.

The first phase of the project is expected to last 27 months, and mobilizes a large research potential. In addition to the €24M ($29.7M) from the European Commission, the partners will also invest advanced research resources to achieve the objectives of the project.

The partners will submit a proposal for the second phase of the NANOCMOS project, starting in 2006, to the European Commission. This phase will aim to demonstrate the feasibility of the 32 and 22 nm nodes. Additionally, the consortium will make a proposal to the MEDEA+ organization to start, in 2006, on the integration and validation of the 45 nm node in an industrial 300 mm wafer fab, currently expected to be the Crolles2 facility, which is jointly shared by Motorola, Philips and STMicroelectronics. These two upcoming project proposals have been integrated in the whole NANOCMOS strategy and discussed with European Commission and MEDEA+ officials.

The project intends to process as demonstrator a very aggressive SRAM chip displaying worldwide best characteristics. This objective will be achieved as early as 2005. The second objective of the project is to realize exploratory research on critical issues of the materials, devices, interconnect and related characterization and modeling to prepare the 32/22 nm nodes considered to be within the limits of the CMOS technologies. The project also intends to process a demonstrator representative of the technology node. This objective will be achieved as early as 2007. The third objective of the project is to take up the demonstration of feasibility results and implement a 45 nm full logic CMOS process integration resulting in the fabrication of chips representative of industrial products in 300 mm wafers. This goal will be achieved before end 2007. This phase will be part of a MEDEA+ project.

For additional information on wafer processing, go to www.semiconductor.net/wafer