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The EUV Train is Still Chugging Away

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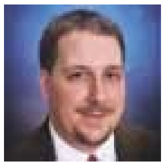
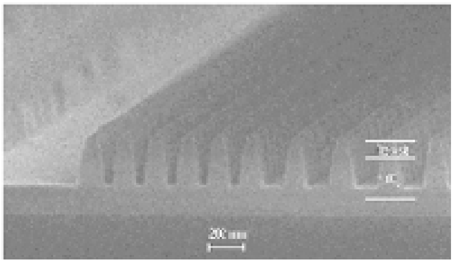


If there's any doubt about whether extreme ultraviolet (EUV) lithography will ever really make it into production, EUV developers are not paying any heed. Announcements have been coming from all directions lately about the progress of the next-generation lithography (NGL) golden child.

CEA-LETI (Grenoble, France) has completed the mounting and alignment of its EUV prototype exposure tool (BEL), and had "first light" in early December. Europe's first EUV exposure tool, BEL will be used in MEDEA+ projects from 2003 to 2005, before alpha tool availability, according to Serge Tedesco, who is leading the lithography team in LETI's silicon technologies department. The tool will be used primarily for early development work on resist processes, he said, and will also be used to evaluate mask technology, and optics and source lifetime studies.

Infineon Technologies (Munich, Germany) announced in November its successful use of EUV lithography to pattern thin dielectric films on silicon wafers (Figure). With an early EUV R&D exposure system in a 120 nm thin experimental resist from Shipley Co. (Marlborough, Mass.), the researchers transferred the patterns into the underlying dielectric film without losing resolution. The wafers were processed at Sandia National Laboratories (Livermore, Calif.).



This SEM shows an as-etched test field processed with EUV lithography, with the resist mask still in place. The narrowest spaces obtained were 60 nm, with a profile height of 160 nm. (Source: Infineon)

The grooves, etched by a plasma etching process, range down to ~60 nm wide. The profile height is 160 nm, which could be considered a first result toward the fabrication of grooves for microprocessors at the 65 nm technology node, the researchers said. Previously, they noted, such structures could only be fabricated with direct-write lithography tools such as e-beam lithography, which has limited throughput.

Also in November, Carl Zeiss SMT AG (Oberkochen, Germany) announced that Exitech Ltd. (Oxford, England) placed an order for two Micro Exposure Tools (METs), optical systems for EUV microsteppers. The end users of the EUV lithography tools will be International SEMATECH (ISMT, Austin, Texas) and an unnamed leading chipmaker. The two-mirror system has a numerical aperture of 0.3 and is designed to achieve a resolution of 50 nm with an image field size of 0.6 × 0.2 mm. Zeiss tested an initial MET earlier this year and achieved a resolution of 50 nm at the first attempt.

Meanwhile, SIGMA-C GmbH (Munich) introduced a software product that simulates each stage of EUV lithography. SOLID-EUV facilitates R&D by allowing users to characterize specifications for masks, mask substrates and lenses. The software enables analysis through aerial images of the exposed, resist-coated wafer surface, allowing users to assess the efficacy of a given process sequence.

And ISMT and Lasertec Corp. (Yokohama, Japan) announced their agreement to jointly develop an EUVL mask substrate/blank inspection system by October 2004. The agreement calls for use of Lasertec's multi-laser beam confocal technology to develop the inspection tool. "Mask blank inspection is a critical-path technology issue in the development of EUVL," said Kurt R. Kimmel, ISMT's mask strategy program manager, in a statement. "In fact, participants in the recent International EUVL Symposium identified defect-free multilayer coated mask blank manufacturing, including inspection, as one of the most urgent issues facing the industry in commercializing EUV lithography.

Selected lithography experts were asked to vote on the key critical issues facing EUV lithography during what was the first International Symposium on EUV Lithography, held in Dallas in October. At the symposium, held in conjunction with ISMT, Europe's MEDEA+ (Paris) and Japan's ASET (Tokyo), experts spent much of the two and a half days assuring each other that, despite critical technical issues still to be completely resolved, EUV technology is indeed heading for commercialization. The top 10 critical issues the industry will face, in order of priority:

- Source output power
- Defect-free multilayer mask blank manufacturing
- Source and condenser optics/reliability
- Cost of ownership of EUV lithography
- Defect-free patterned mask manufacturing and commercial availability
- Reticle defect protection
- Effective contamination control of optical path
- High-NA optics manufacturing
- Thermal management for reticle and projection optics at high throughput
- Simultaneously achieving resolution, sensitivity, line edge roughness and low outgassing for commercial EUV photoresists

The semiconductor industry is aiming for 2007 to have EUV lithography ready for prime time. There is still a lot of work to do to get there, but developers seem determined to get it done.

For additional information on lithography, go to www.semiconductor.net/lithography.