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Space particles hit logic chips

By Chris Edwards, EE Times UK
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Radiation from space is becoming a chip design issue, as feature sizes shrink and chip frequencies increase to the point where logic circuits as well as memories become prone to switching unexpectedly when hit by neutrons or alpha particles. No-one is certain how bad the problem is or how quickly logic circuits are affected already. Measured as failure in time (FIT) — caused by single-event upsets and transients — the publicly available data for logic is sketchy.

Both the International Technology Roadmap for Semiconductors, published by the US semiconductor consortium Sematech, and the Medea+ design automation roadmap have called for more research into how badly logic and memory will be affected in the future by radiation.Eric Dupont, president and CEO of French radiation effects specialist Iroc Technologies, said: "There isn't accurate data on FITs per kilogate. So we are launching a partnership on 130 and 90nm, and we will have results next year."

The company has put together a set of test chips with a small group of unnamed companies to try to get closer correlation between simulation and reality with single-event transients and events. Iroc is now trying to recruit more companies with a programme, Sertest Shuttle, that mirrors the Silicon Shuttle multi-project wafer trial system operated by foundry TSMC.

Don MacMillan of Synopsys says there has been little evidence up to now of logic problems, although on-chip memory is now incorporating radiation protection schemes.

He said: "On the data I've seen, it is inconclusive whether logic is going to be a real issue with single-event upsets. That is partially because gate delays will filter out some of the induced glitches. We need to see if there is new data.

"In general, unless it's dynamic logic — if it's just CMOS [static] logic — it's just another glitch. And synthesis produces a lot of glitches anyway. The sensitivity is around your latch time."

Dupont says Iroc's work will provide a view of logic sensitivity as well as that of memory. Without the test chips, the absolute FIT probability of a circuit in a given process remains uncertain, he says, but there is a clear trend from simulations.

"There is a linear increase in sensitivity with clock frequency," said Dupont. "Errors created will be more and more latched as circuit frequency increases."

The test chips will let Iroc calibrate its simulations, says Dupont. "We want to see the pulse width and the critical charge."

Radiation sensitivity has long been a concern for those working with discrete memory chips. It is a major driver behind the use of error-correcting circuits in servers and network equipment. Now, FIT probability is becoming a measure employed by those selling memory intellectual property (IP) for use in system-on-chip (SoC) designs.

Dupont said: "Customers are beginning to compare the FIT rate of each memory as well as speed, power and area."

MacMillan added: "Error correction has to be built into on-chip memories. Particularly in network chips, it is mandatory at 130nm and probably at 180nm. All the high-end users are using it and it will filter through to the other guys."

But some logic IP suppliers such as ARM Holdings are understood to have begun work on analysing the sensitivity of future cores as concerns loom over reliability during e-commerce transactions.

For on-chip memories, a big concern among chip designers is the emission of alpha particles by flipchip solder bumps. IBM Microelectronics presented a paper at the recent Custom Integrated Circuits Conference on techniques to reduce the FIT probabilities in on-chip memories. In many cases, it means moving or deleting bumps over the memory cores.

Cadence Design Systems aims to use this kind of information in future flows that couple chip and package design.

Lavi Lev, general manager of IC implementation for Cadence, said: "You need two things. One is smart placement of I/O pads and the other is the use of circuit techniques to avoid radiation effects."