MEDEA+ and ENIAC set Europe's nanoelectronics agenda

by Brian Dance, contributing editor, Europe

Pan-European collaborative R&D presented at the recent MEDEA+ Forum (Nov. 28-29, Monte Carlo) showed that the nations of Europe are determined to remain among the world leaders in nanoelectronics, which is regarded as a driver for their economic growth. Four hundred partners from 22 countries have already invested 18,000 person-years in 75 MEDEA+ projects exploring technologies and applications, 44 of which have been successfully completed.

Following on from the MEDEA program in 2001, MEDEA+ will run until 2008, channeling private and public funding into microelectronics R&D. A successor program, Beyond MEDEA+, will be under the strategic research agenda of ENIAC (European Nanoelectronics Initiative Advisory Council), whose mission is to combine visions and R&D efforts from European research centers, semiconductor manufacturers, equipment and materials suppliers, end-users, and government and academic authorities to foster a truly competitive European nanoelectronics industry.

Several projects currently under MEDEA+'s watch involve leading-edge technologies and materials for process nodes below 65nm, such as strained SOI, 300mm/45nm transistor architectures, and nonvolatile memory, as well as methods to improve chip production methods that are closely attuned to Europe's semiconductor industry.

The "SilOnIS" project (#2T101), begun in Jan. 2005 and running until Dec. 2007, aims to provide an industrial source of large diameter strained SOI wafers for high performance ICs, combining SOI architectures with advanced forms of strained silicon to achieve improved carrier mobilities, better transistor I_{on}/I_{off} ratios, etc. Results at the halfway stage include the demonstration and sampling of thin (fully depleted SOI) and thick (partially depleted SOI and FINFET) 300mm strained SOI (sSOI) substrates. Significant sSOI material improvements have already made the materials competitive with a typical defect density of 0.2 defects/cm^2, while the best wafers have <0.07 defects/cm^2. FD SOI devices with 25nm gates and a TiN/HfO_2 gate stack have been produced. SilOnis project partners include Si-based substrate suppliers (Soitec and Siltronic), equipment suppliers (ASM and AIXIRON), IC manufacturers (Crolles 2 Alliance), and specific metrology equipment suppliers (Horiba, Sopra, OMI, Accent).

The "FOREMOST" project (#2T103, Jan. 2006-June 2008) is developing advanced process modules and transistor architectures to demonstrate 45nm CMOS process technology in European 300mm production by 2010, targeting both CMOS logic and DRAM/flash memory technologies, and promoting synergy between the competencies of the Crolles Alliance (STMicroelectronics, Philips, and Freescale) and Infineon. The project will employ 193nm immersion lithography, but will also assess the potential of nanoimprint lithography for a specific metal level of the multilevel interconnection process. High-*k* metal gate dielectric structures based on new materials will enable equivalent oxide thicknesses of <1.5nm. Led by STMicroelectronics with 22 partners, FOREMOST aims to let manufacturers propose the most advanced logic technologies ahead of ITRS predictions to boost European industry, directly impacting high complexity component performance and reducing cost per function.

Another MEDEA+ project, "HYMNE" ("High Yield Driven MaNufacturing Excellence, #2T102, Feb 2005-Dec. 2008), aims to develop software and hardware methods that will help shorten production cycle times and improve device -- an area that is particularly important in Europe, where much production is based on short-run application-specific products. HYMNE sets out to show cycles can be shortened for <65nm devices with yields of >78% within 13 months of first silicon, and aims to reduce cycle times from two days to one day per mask layer, and from 0.75 to 0.35 days for fast prototyping in a 300mm operation. This project runs under the leadership of Joost van Herk, Philips.

Reducing the time needed to validate novel non-volatile memory (NVM) cell concepts and process options is the focus of the "NEMeSyS" project ("Nonvolatile Embedded Memories for Systems on Silicon, #2T201, Jan 2005-Dec 2008), which hopes to secure a competitive position for Europe in embedded applications such as global telecom and wireless communications, smart card, and consumer and automotive electronics. The work is particularly important to MEDEA+ partners generating innovative SOC techniques for rapidly expanding markets, e.g. sub-100nm CMOS, where feature density, performance, size/weight ratio and cost are vital factors that can be met only by higher levels of integration with embedded NVM. NEMeSyS partners led by Philips NL still consider stacked gate NVM the technology of choice for 65nm and beyond, with questions still surrounding alternative technologies such as FeRAM, phase-change memory, and magnetic RAM, although R&D on innovative cell options such as SONOS will bring these closer to industrialization.

Successes already achieved in extreme ultraviolet (EUV) lithography from completed projects masks, sources, and photoresists are now benefiting manufacturers, and the "EAGLE" project ("EUV Advanced Generation Lithography in Europe," #2T301) aims to develop technology for a EUVL platform that will enable volume IC production for the 32nm node in 2009, as per the *ITRS* roadmap. Key subsystems of the lithographic tool will be integrated in the project to demonstrate the feasibility of the system and technology target specifications. EAGLE follows the work completed by the three-year More Moore project, which had been led by ASML to promote the development of extreme ultraviolet lithography (EUVL) in Europe.

The "MUSCLE" project ("Masks through Users Supply Chain: Leadership by Excellence," #2T302) is working on controlling mask costs and safeguarding European autonomy in masks for nanoelectronics. IC designers, maskmakers,

material providers, software houses, and mask users are combining to create a leading-edge supply chain for highly advanced, zero-defect quality masks.

Reportedly led by CEA-Leti, the "FANTASTIC" project (Full Assessment of Nano-imprint Technology Addressing Sub-35nm ICs, #2T305) aims to establish and assess a step-and-repeat UV-based nanoimprint lithography infrastructure for CMOS 32nm node requirements. This will create a running "virtual" infrastructure including all aspects, such as imprint tool development and template fabrication including metrology repair processes, as well as process development and metrology. -- *Brian Dance, contributing editor, Europe*