Samsung Electronics has created the first LCD panel that can produce independent images on each side of a mobile LCD display. Samsung's new double-sided LCD can show two entirely different pictures or sets of visual data simultaneously on the front and back of the same screen. Other conventional double-sided LCDs can only show a reverse image of the same video data. This new development is expected to replace two display panels with one, thereby reducing overall thickness of mobile products by at least 1mm. Samsung has based the new technology on its proven double-gate, thin-film transistor (TFT) architecture.

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A technique which will allow silicon wafers to be stacked accurately and inexpensively in 3D structures has been developed by researchers at the University of Southampton.

To date, the major challenge when stacking silicon wafers has been to align one wafer to another, matching all the features. At the moment, big machines are being used and the process is being carried out optically, with a path that is long and introduces errors.

At Southampton University, however, researchers have used a passive alignment technique and achieved alignment as precise as 200nm. The alignment features consisting of convex pyramids and concave pits can be fabricated and chip scale specimens can be successfully bonded after the microfabrication process.

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NEC Electronics has introduced a 55nm cell-based IC, with a significantly lower power consumption, suitable for portable devices.

The cell, CB-55L, is based on NEC's UX7LS process technology, which demonstrates a 40% power reduction from the previous 90nm CB-90M cell. CB-55L also offers more than double the density of previous devices and offers very high reliability by resolving parameter variations often encountered at advanced process technology nodes.

Other of the cell's features include high reliability, reduced turnaround times and a comprehensive IP library optimised for portable devices. IP macros such as USB2.0, JPEG, DDR/DDR2 required for digital cameras, camcorders and other battery-operated applications will also be added to the device.

IMEC develops germanium PMOS devices

IMEC, the Inter-University Microelectronics Centre in Leuven, Belgium, has investigated the use of germanium for future pMOS devices of nanoscale dimensions. It provides a high mobility channel material that is said to be potentially better than strained silicon, but previous results using it have been limited to either long channel or to ring shaped devices.

IMEC has employed enhance-ment techniques, including strain, to obtain excellent hole mobility in long channel devices of up to 2.7 times higher than the universal hole mobility in silicon and high drive currents for short channel devices. The shortest gate length was reported as 125nm.

IMEC fabricated the pMOS devices by using a silicon compatible process with 200mm diameter germanium on silicon wafers made by ASM. The uppermost germanium layer on the wafers was deposited by epitaxial growth directly onto the silicon. An extremely thin 0.6nm epitaxial silicon layer, partially oxidised after its formation, provided passivation for the germanium surface. The silicon passivation layer was immediately capped by a 4nm thick dielectric layer of hafnium oxide deposited by using an ASM Pulsar reactor, which was followed by a 10nm layer of tantalum nitride and an 80nm layer of titanium nitride deposited by physical vapour deposition.

The effective oxide dielectric thickness was only about 1.2nm resulting in a gate leakage less than $0.01A.cm^{-2}$. In a typical device of dimensions 10 x 10µm, a peak carrier mobility of $315cm^2/Vs$ was achieved. The drain current of 670µA per micron is claimed as a record for a gate length of 190nm and a Vd of –1.5V.

IMEC intends to further improve the device performance by implementing strain, optimising the ion implantation and reducing the gate length even further. The results, reported at the IEEE International Electronic Devices Meeting in San Francisco, California, are part of an IMEC core programme on sub-32nm CMOS in collaboration with the companies Infineon, Intel, Micron, NXP, Panasonic, Samsung, ST Microelectronics, Texas Instruments and TSMC.

FOREMOST project will integrate 45nm CMOS technology

A MEDEA+ project known as FOREMOST aims to maintain the European lead in CMOS IC manufacture by developing and demonstrating advanced process modules and transistor architectures. These will include a full 45nm mode technology for use in industrial 300mm wafer fabrication plants by 2010.

Running from January 2006 until June 2008, the project incorporates both CMOS logic and DRAM/Flash memory technologies. Currently, the major manufacturers mass produce DRAM memory chips with 90nm node technologies.

The DRAM work in FOREMOST aims to develop new devices for the peripheral transistors required for future double data rate standards and novel transistor structures for DRAM cell arrays. The arrays are related to new CMOS logic that will require three dimensional structures in due course. FOREMOST intends to let manufacturers propose the most advanced logic techniques even ahead of the International Technology Roadmap for Semiconductors (ITRS) predictions to boost the European industry. It will directly impact high complexity component performance and reduce the cost per function.

A process ready for integration is expected to be achieved by the middle of 2008. The project involves 22 partners from eight countries.