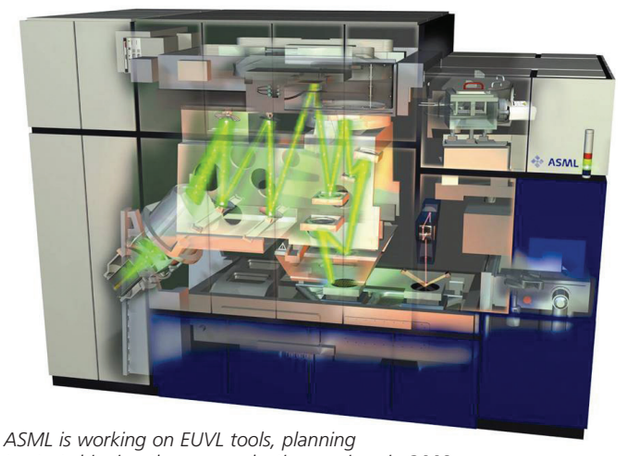
EAGLE for EUVL

A new MEDEA+ project named EAGLE aims to develop an Extreme Ultra Violet Lithography (EUVL) platform for volume manufacture, which is expected to serve for the next decade. It will enable industry to produce ICs for the 32nm node in 2009, as in the ITRS roadmap.

Lithography tool manufacturers have now decided that the source power for EUVL tools providing a throughput of 100 wafers per hour should be 180W at the Intermediate Focus (IF) for resists that require a 10mJ/cm^2 dose. MEDEA+ R&D results are now being used to develop EUVL tools towards the required power level. The latest research by ASML with Sn sources, in terms of power output, debris control and spectral purity, suggests that such sources are scalable to the required power level for production systems within about two years. However, continued work on source reliability will be needed. This time-frame also depends on many other factors, such as the readiness of EUV reticles and resists.

Relatively new Sn source technology limits current power to 20-50W at the IF. ASML has supplied two alpha demonstration tools to research partners which will be qualified on site with Sn-based sources in 2007. Sources in the past were based on Xe, which do not seem to be scalable to the 180W required at the IF. ASML plans to ship pre-production EUVL tools in 2009, followed about two years later by systems that can meet the desired 100 wafers per hour level. Laser plasma sources are potentially able to provide adequate power, but are not cost-effective, so research has concentrated on discharge plasma Sn sources. ASML says that it is too early to firmly predict the precise type of source that will be used in future systems, but work with laser triggered, multiplexed Sn sources is very promising in terms of the power produced, the heat load and electrode erosion.



ASML is working on EUVL tools, planning to start shipping the pre-production versions in 2009

Non-volatile on-chip re-programmable memory technology from Europe

A Non-volatile Embedded Memory for Systems-On-Silicon (NEMeSyS) project will develop embedded Non-Volatile Memory (NVM) technology for integration into standard baseline CMOS technologies. The emphasis will focus on NVM electrically erasable and programmable read-only memory, such as Flash and EEPROM, to create programmable product platforms for system-on-chip realisation.

This MEDEA+ 2T201 project will enable the industrial MEDEA+ partners to generate innovative techniques for rapidly expanding markets. They are expected to be especially useful in the previously unavailable field of sub-100nm CMOS, where feature density, performance, size/weight ratio and cost are vital factors that can be met only by higher levels of integration with embedded NVM.

Programmable on-chip NVM enables the same chip to be adapted to various applications, thus greatly reducing costs and addressing the paradox between low volume system-on-chip products and mass production. NVM tunnel oxide and programme/erase voltages do not scale satisfactorily, so they are posing increasing problems with each new generation of yet smaller devices. Stacked gate NVM is still considered the technology of choice down to 65nm and less, but is expected to become more and more difficult to realise with smaller features. Thus, the main challenge will be the scaling of stacked gate technology for new device generations. Hence, a decision has to be made about the possible implementation of other technologies, such as magnetic RAM that could be potentially useful. R&D on innovative cell options, such as Silicon Oxide/Nitride/Oxide/Silicon (SONOS), will bring these closer to industrialisation.

A reduction of the time needed to validate and industrialise novel NVM cell concepts and process options is required to ensure European companies are competitive in global telecommunications, wireless communications, smartcard, consumer and automotive electronics. Global competition comes from the US and Far East, especially for NVM applications in the smartcard, consumer and automotive sectors.

The project started in January 2005 and is scheduled to run until December 2008. It is led by Frans List of Philips, The Netherlands, with other partners being Atmel, CEA-LETI, IMEC, Infineon Technologies and STMicroelectronics. The technology options being developed will be transferred to the production sites used by the partners.