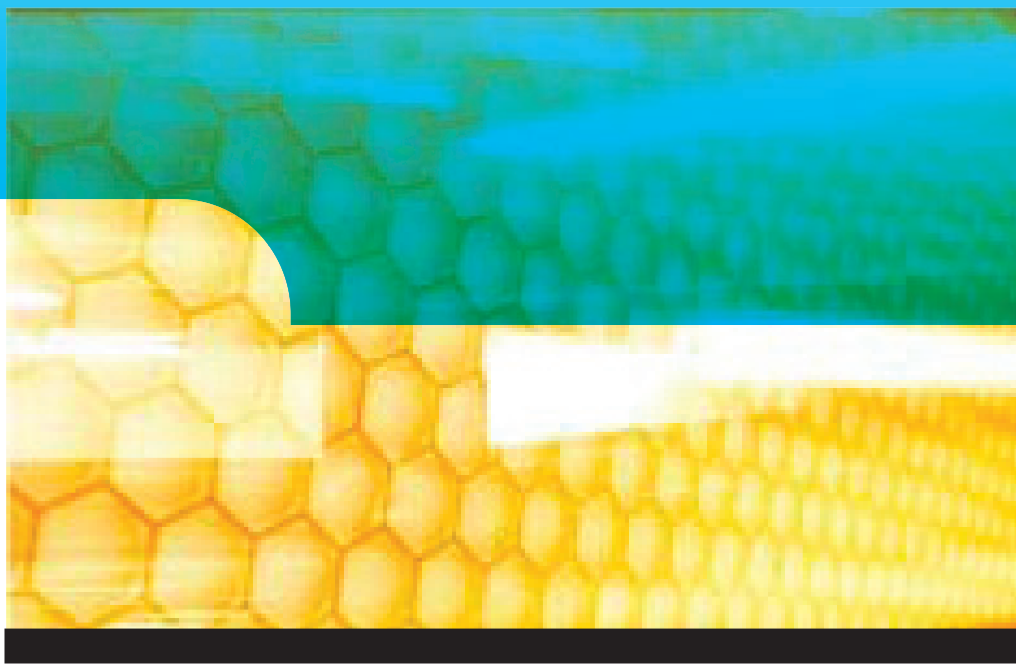
Excerpts from MEDEA+ Phase 2 / CATRENE

2010 Assessment



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Preamble

In May 2010, the CATRENE Public Authorities Director's Committee (CDC) jointly requested an assessment on MEDEA+, Phase 2 / CATRENE, as part of the preparation for a decision of an extension of CATRENE beyond 2011.

The purpose of the assessment is:

- **To highlight the main achievements on the programme and project level**
- **To verify that these projects have created commercial success; were technically appropriate and used reasonable budgets**
- **To verify whether the programme as a whole has lined up to its goals and expectations as formulated at the beginning of MEDEA+ phase 2/CATRENE.**
- To give some recommendations on how to increase the programme's efficiency.

Due to the short time available to carry out the assessment the Public Authorities suggested the details of the report were worked out within the CATRENE Office and then the results and conclusions were audited and verified by an independent **expert, namely Future Horizons, a well known semiconductor consultancy based in the UK.**

EXCERPTS OF
FUTURE HORIZONS REPORT

Executive Summary

Introduction

This Report summarises the results of Future Horizons' October 2010 independent expert audit of the CATRENE office MEDEA+ Phase 2 and CATRENE Programmes Assessment Report.

For the past two decades, the EUREKA JESSI (1989–1996), MEDEA (1997-2000), and MEDEA+ (2001-2008) programmes have made it possible for Europe's industry to reinforce its position in semiconductor process technology, manufacturing and applications, and in so doing to become a key supplier to key world markets such as telecommunications, consumer and automotive electronics, whereby European industry has today successfully:

- Conquered vital high technology domains through technical innovation;
- Learned horizontal and vertical co-operation; and
- Produced several globally successful industrial champions.

As a result, Europe has achieved a 20 percent world market share in Information and Communication Technology (ICT), an achievement that many pre-JESSI saw as hopeless. Within this, semiconductors have become one of the strongest European ICT segments, underpinning the achievements in all of the other sectors.

In order to further enhance European ICT competitiveness, a follow-on programme, CATRENE, was started in 2008 with the vision to achieve **"Technology Leadership for a competitive European ICT industry"**.

CATRENE is a four year programme, starting 1 January 2008, but extendable by another four years through 31 December 2015. In the period covered by this evaluation, CATRENE labelled 24 projects, of which 17 were looked at in detail, the other 7 having been cancelled after labelling for reasons outside of the control or influence of the CATRENE organisation. Most of these projects are still ongoing and the results anticipated cannot yet be measured. All projects of MEDEA+ Phase 2 were analysed as to their usefulness and purpose, although some are still ongoing.

Future Horizons believes Europe has every right to be justly proud of its collective achievements and we strongly believe that continued public support is the right approach for the next phase of CATRENE. Based on the results achieved to date, industry has clearly paid back the trust and commitment implied by receiving public investment and we have no hesitation in recommending a follow-on nanoelectronics support programme once the current CATRENE programme ends in 2011.

Summary Of Conclusions

- MEDEA+ Phase 2 and CATRENE's goals are in line with both Europe's strategic needs and the general development of the globalised nanoelectronics world. The achievements to date show an impressive range of results and the projects are in line with the ITRS roadmap or with state-of-the-art research activities;

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- Many of the MEDEA+ technology projects have been highly significant. For example the FOREMOST project commercialised the 45nm CMOS technology developed in the ESPRIT NANOCMOS project. 2T301: EAGLE and 2T304: LIQUID and other projects maintained European strength in advanced lithography (worldwide market-share >70 percent), whilst other projects covered topics such as advanced non-volatile memories, power devices, microwave devices and chip/package co-design. Looking at the whole list every project appears to have an obvious commercial advantage in their specialist area. Since many projects are completed quite recently, we expect more results to be made available soon. We believe that in all projects there is a fair balance between input in terms of person-years and results achieved;
- Europe now matching best in class in SOI and supplying >70 percent of the world's SOI wafers.
- Mature 3D integration technology platforms and innovative packaging SiP;
- MEDEA+ and CATRENE provide a platform for joint development, competences and standards, both horizontally and vertically within the supply chain. Examples are the demonstration of European solutions and standards for security and trusted computing. European smart card and security activities have created standards and technologies as enablers for new applications and secure services, dominating the global smart card market. In the trusted computing field, which is dominated by USA, the TSC project has created a European solution of key strategic importance;
- MEDEA+ is a real success story: essential breakthroughs have been achieved in a number of applications related to wireless broadband, multimedia systems (BluRay standard) and terminals (3DTV); essential contributions to automotive platform development, substantial achievements in reliability, safety and intelligent features for vehicles;
- MEDEA+ strongly advocates for more Electronic Design Activities in Europe. After releasing the first EDA roadmap in 2005, a new one was edited by CATRENE in 2009. It can be used as a yardstick for further activities. The roadmap is also well recognised by the ITRS organisation. Some EDA SMEs have achieved unique breakthroughs in e.g. simulation time reduction by intelligent data reduction;
- It is obvious, that the time span between time of labelling a project and real start date has to be significantly reduced, even more for bottom-up projects. The pace of change and technological development in the information economy is so furious that even a small delay in exploiting a commercial advantage, or technological invention, can mean millions of euro in lost sales and profits, and even the loss of the market itself.
- We believe CATRENE has adequate selection criteria in place during labelling, and appropriate project reporting and monitoring procedures in place to ensure the continuing high quality of the projects.

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- We are totally supportive of CATRENE as a concept and view the vast majority of current projects as valid, a good investment of public funds and capable of creating commercial opportunities for European companies.

Summary Of Recommendations:

- MEDEA+/ CATRENE played a decisive role for the value chain in nanoelectronics. Since nanoelectronic is a key enabling technology (KET) for Europe and the driving force for the development of future goods and services affecting almost all parts of our life, a strong position is key for European competitiveness. CATRENE has a unique position in relation to national and other supra-national R&D programmes due to its industry led bottom-up approach. The public authorities involved in CATRENE should therefore continue to support the second phase of CATRENE;
- We believe that if the companies released more information on the commercial success of products that incorporate projects funded under CATRENE then fewer doubts would be expressed on the effectiveness of the programme. We suggest this is made a condition for participation in CATRENE projects;
- There are several examples of SME success stories in the MEDEA+ programme. These should be published more clearly as a demonstration for other potential SME participants;
- CATRENE will have to master both 'More Moore' and 'More Than Moore' technologies. Without support for such advanced CMOS technologies, Europe will simply cease to be a player in advanced semiconductor wafer fabrication;
- The public authorities need to change the national approvals process to a parallel rather than serial process so that funds are released as soon as a project is approved by CATRENE.

1. INTRODUCTION: "ROOTS OF PROSPERITY"

The European Councils of Lisbon and Barcelona set out clear economic goals for the Community: "Within 10 years the European Union will become the most dynamic and competitive knowledge-based economy."

For consumers, this means new products and services that combine high added value with competitive pricing. At home, we want solutions that genuinely improve our quality of life. On the move, we want to stay in touch anytime, anywhere, for business or private reasons.

In addition to driving industrial and consumer markets, advanced electronics is crucial to the public sector because of its power to deliver key social benefits such as security, health and welfare, education, as well as an efficient and respected public administration.

For the wider community to receive such benefits, industry needs to maintain a high rate of innovation for products and services, supported by advanced manufacturing techniques, all backed by fast and reliable data management.

This dynamic and competitive future requires user-friendly solutions; products that conceal huge amounts of processing power, providing users with 'simple to use' devices – not requiring manuals or training - but 'complex on the inside' from advanced microchip engineering.

There has been a fast and strong evolution in semiconductors that comprise the building blocks of innovation: both the processing power and available features on new microchips have increased dramatically, while their size and price have decreased in proportion. Today the 'micro' of microelectronics is being shrunk into silicon chips measured in billionths of a metre (nanometres).

This is the world of nanoelectronics. It makes possible a new generation of advanced devices with easy to use features that conceal great complexity – thanks to a new ability to reconcile the demands of space, power and cost. These tiny nano-chips with power pervasive networks of miniaturised devices provide consumers with solutions previously only affordable by large companies.

Nanoelectronics technology has an impact beyond the world of consumer gadgets. It will support Europe to accomplish a better life style with the lasting wellbeing, stability, comfort and safety that citizens demand and deserve. It is an efficient, cost-effective route to achieving the European goal of prosperity within a strong social structure. Tomorrow's consumer goods, industrial processes and improved systems for collective health, education and welfare will all develop from a solid base in nanoelectronics.

With the groundwork so promisingly laid, it is inconceivable that Europe could allow such great opportunities be transformed into threats. Now is the time to make a positive choice if we hope to use advanced technology to help us to realise our aspirations for the future.

So we stand at a cross-road; experience gives us confidence that we will once again choose the right road and repeat our past successes, but on a larger and even more ambitious scale. Yet, this will only happen if Europe opts to continue a bold programme of coordinated R&D investments to create more industrial clusters and 'eco-systems', creating and safeguarding tens of thousands of jobs in Europe.

Europe is engaged in a high-stakes industrial competition to guarantee its future as an innovative, prosperous and knowledge-based community. The private sector will play its part, but the public sector must join in a full-scale public-private partnership aimed at safeguarding a common destiny in the global race between regions.

2. CO-OPERATION IN EUROPEAN MICRO-/NANOELECTRONICS R&D

The Joint European Submicron Silicon Initiative (JESSI), the first EUREKA cluster programme in microelectronics, represented a fundamental restructuring in the European electronics and information technology industry. Europe not only built up world class submicron semiconductor capabilities, but also an effective continent-wide infrastructure for collaboration. Since then, follow-on programmes were launched as part of the EUREKA initiative; MEDEA, MEDEA+ and then CATRENE, complementing the Framework Programmes of the European Commission and more recently the Joint Technology Initiative ENIAC, and backing up the industrial efforts both politically and financially.

These programmes, widely recognized as successful, did more than provide indispensable financial support: they played a pivotal role in anchoring the key-enablers in Europe for almost all technical advances of the industrial society and successfully managing ever changing landscape and challenges in this high-tech segment.

It would however be wrong to believe that – after having achieved a prosperous position in the worldwide competition in nanoelectronics or semiconductors – industry can focus solely on the exploitation of results achieved to date.

Furthermore even more complex challenges have to be mastered to be the champions, including the following:

- Geographically, in addition to Europe, US and Japan, there are new production locations in Taiwan, Korea, Singapore and most recently China, representing together a market share in excess of 50% of the world.
- European companies have successfully managed to play in the top champion's league of worldwide semiconductor and equipment suppliers in some specific but major application segments, but they have to defend their ranking.
- In line with ITRS, European IDM companies have introduced successfully 65 and 45 nm node technology and will introduce 32 nm and most advanced technology at 22 nm and below, but they are not the leaders in the More Moore technologies.
- The European Commission is rating nanoelectronics as a key enabling technology and thus a European strategic segment.
- Today electrical or electronic components represent around 20% of the value of an electronic equipment, compared to 7% 25 years ago.
- The business model fablight/fabless, first introduced in the USA region, is now offering new possibilities to European companies, in addition to the vertically integrated IDM businesses.
- Quite recently, Europe managed to become an interesting region for new investors: the Abu Dhabi government decided to expand the semiconductor foundry activities to Europe as well.
- In addition to the French mega-project "Nano 2012," France will invest 1-2 b€, to become one of the top 5 countries in nanoelectronics.

IT CAN BE SEEN THAT NOTHING IS SO PERSISTENT AS "INNOVATION"

Europe can not stop to manage upcoming changes in the technical evolution. On the contrary, it has to manage the challenges of societal needs and to master technology innovations. Even if R&D costs for next system-generations are in excess of the capabilities of even the largest industrial conglomerates, and even in excess of some countries' possibilities, Europe has to maintain access to the latest technological evolutions in nanoelectronics. It has to defend its economic independence. Europe needs the continuation of the precompetitive research in nanoelectronics within the CATRENE cluster programme beyond 2011.

In preparation of a decision on such an extension, Public Authorities are requesting an assessment on MEDEA+ phase 2/CATRENE.

MEDEA+ Σ! 2365 (MicroElectronics Development for European Applications) is the industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis. The programme had a time span of 8 years (2001 – 2008) and had a mid-term assessment at the end of phase 1 (2001 – 2004).

CATRENE Σ! 4140 (Cluster for Application and Technology Research in Europe on Nanoelectronics) will foster Technological Leadership for a competitive European ICT industry. It is the ambition of Europe and the European Companies to deliver nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and establishing its industry at the forefront of the global competition.

CATRENE is a four-year programme (2008 – 2011), started 01 January 2008 and is extendable by another four years. This is in line with the changing landscape of the semiconductor industry as well as the present views on technology evolution and the time span, over which most of the major applications will be developed.

During 2008, both programmes MEDEA+ (2nd phase) and CATRENE (1st year) ran in parallel to avoid any start-up problems and to ensure the continuity of these key EUREKA programmes.

With the advent of the ENIAC JTI, the PPP landscape changed. This Joint Technology Initiative launched by the EU and Member States represents the nanoelectronics R&D activities in a similar manner to the CATRENE programme.

Because of this, CATRENE and ENIAC organise during each year several common events, e.g. brokerage events, European Nanoelectronics Forum, et alia. CATRENE and AENEAS (Industry association of ENIAC) also have common meetings with Public Authorities.

The differentiation between the two programmes can be seen in their respective approaches - ENIAC is top down whilst CATRENE is bottom up - and the type of projects as described in the delineation paper. This delineation is a pragmatic approach to help Industry and Public Authorities to decide which instrument is the best for supporting projects and policies in CATRENE and ENIAC. These two programmes on nanoelectronics aim at strengthening the competiveness of Europe and its industry, offering innovative solutions for Europe at large.

Delineation will not prevent effective links between themes in both ENIAC and CATRENE when appropriate. A limited overlap can be also desirable for flexibility. The two instruments (CATRENE and ENIAC) will be governed by one common strategy with a corresponding delineation and strategic prioritization of both programmes.

Nevertheless, due to the fact that the Public Authorities did not structurally increase their budgets for this industry, CATRENE sees a number of consequences of the coexistence of the two programmes, e.g. less projects, less funding, etc. More details can be found in chapter 3.3.

When comparing the two approaches CATRENE is the recommended tool for multi-disciplinary and multi-cluster projects. The bottom up approach and the flexibility of CATRENE is well adapted to allow new activities and innovations from various scientific domains to be embedded in nanoelectronics devices or to be adapted for semiconductor activities.

The ENIAC's top down approach reflects priorities at the European level for the benefit of a large number of European countries. ENIAC cannot replace the EUREKA bottom up approach of CATRENE. The ENIAC projects should be dedicated to addressing the "Grand Challenges" for Europe. Based on the concept of flexibility and in its open mindset, CATRENE therefore is not restricted to the Grand Challenges. ENIAC and CATRENE are complementary and not competing initiatives.

Conclusions

Since the beginning of CATRENE in 2008 there have been many changes in the environment in which the programme operates.

- General financial and economic turmoil in late 2008, 2009 and 2010 has negatively influenced and impacted all domains, including that of the ICT, and Government intervention and stimuli have accelerated changes and recovery in the various regions.
- Semiconductor industry development faced short term challenges with global economic meltdown in 2008 and 2009. Industry reacted quickly and the long-term prospective continues to remain promising as advanced technology continues to bring benefits to consumers and business worldwide.
- The microelectronics sector is particularly globalized through alliances, international ownership of corporations, re-location of manufacturing and R&D, and so on. The question of whether there is a European industry creating added value and wealth in Europe is becoming a more precise topic and political issue, which also affects the political support to CATRENE. The sense of urgency regarding the competitive position of the European microelectronics industry that was evident at the launch of JESSI and MEDEA, is not as obvious today, despite the recognized strategic importance of silicon technology.
- CATRENE is the recommended tool for multi-disciplinary and multi-cluster projects. The bottom up approach and the flexibility of CATRENE is well adapted to fit all new activities/innovations issued from various scientific domains to be embedded in nanoelectronics devices or to be adapted for semiconductor activities. The Joint Technology Initiative (JTI) ENIAC launched by the EU and Member States cannot replace the EUREKA bottom up approach of CATRENE. The ENIAC top down approach reflects priorities at the European Level for the benefit of a large number of European countries. The ENIAC projects should be dedicated to addressing the "Grand Challenges" for Europe whilst with its concept of flexibility and open mindset, CATRENE is not restricted to the Grand Challenges.
- The two instruments (CATRENE and ENIAC) should be governed by one common strategy with a corresponding delineation and strategic prioritization of both programmes. In this view CATRENE addresses mostly Technologies and challenges involving fewer Member States and/or partners. A merge of both programmes is thus not recommended and an extension of CATRENE is the preferred route forward.
- Nothing is so persistent as the race for "Innovation." Europe cannot stop to manage the challenges of societal needs but has to master new innovations. Europe has to maintain access to the latest technological evolutions in nanoelectronics in order to shape its future on time and defend its economic independence. Europe needs the continuation of the pre-competitive research in nanoelectronics as in the CATRENE cluster programme, beyond 2011.

3. MEDEA+, PHASE 2 & CATRENE, KEY FIGURES AND STATISTICS

3.1 Time Schedule

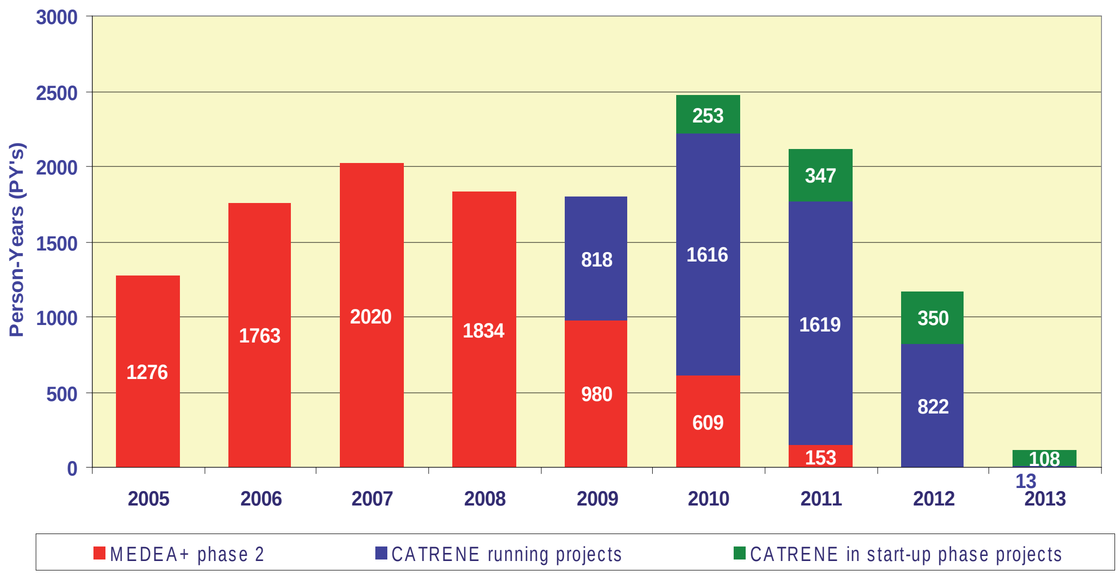
Despite the expiring MEDEA+ programme at the end of 2008, MEDEA+ labelled projects that had not yet ended are continuing their activities until their intended completion dates, with some of them running until year-end 2011. The respective project monitoring and reporting activities will be ensured and undertaken within the frame of activities related to the successor programme CATRENE. The data used in this assessment are taken from the MEDEA+/CATRENE database as of beginning of September 2010.

MEDEA+ stakeholders decided at the beginning of the programme, that the average level of resources funded in labelled projects should be around 2500 – 3000 persons per year. The respective cost volume corresponds to about 500 M Euro per year.

In figure 1 below, MEDEA+ phase 2 is reflected in red colour, CATRENE running projects in blue colour, and CATRENE start-up projects in green colour. One year after labelling there are still a substantial number of call 2 projects in a start-up mode.

It should be taken into account that some of the running projects, even more the projects in start-up phase, are subject to changes in terms of person-years involved and sometimes even in partners. CATRENE call 3 is still in the evaluation phase and is therefore not shown.

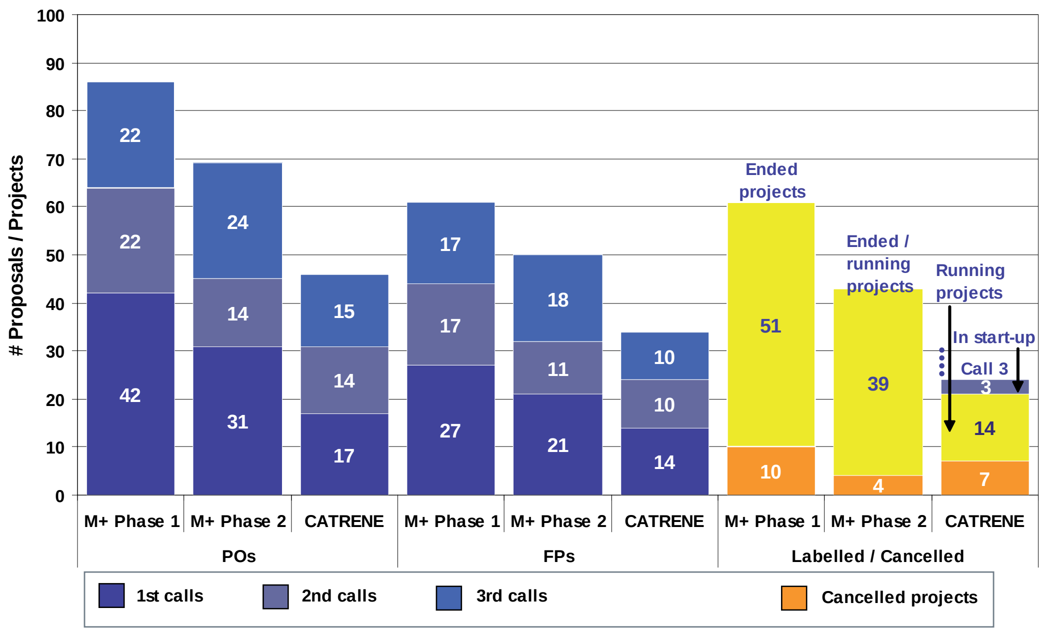
Figure 1:
Time Schedule



3.2 History of Calls for Proposals

A very comprehensive statistic is shown in figure 2, the summary of "Calls for Project Proposals" of MEDEA+ phase 1, MEDEA+ phase 2 and CATRENE. In all three intervals there have been 3 calls, therefore the scenarios are quite comparable.

Figure 2:
Calls in MEDEA+ / CATRENE



In the left block of the figure, there is the summary of received proposals at the stage of the project outlines (PO's). The three calls are shown as columns with different intensity of colours, call one always on the bottom of the column.

In the middle block of figure 2, the same set of information is given for the stage of full proposals (FP's).

The reduction of project proposals at the FP stage compared to the stage of PO, reflects roughly the same quota in all three intervals, i.e. 71%, 72%, 74%, and is thus in line with normal procedures and experience gained.

In the right block of the figure, the labelling and cancellation policy is visible: in MEDEA+ phase 1, all 61 FPs have been labelled however, 10 labelled projects have been cancelled, as they never started.

In MEDEA+ phase 2, out of 50 FPs only 43 have been labelled and later 4 of the 43 projects have been cancelled, as they never started.

In CATRENE, the labelling process of call 3 will be done in two steps, at the end of June and towards the end of 2010. It is therefore only referred to the situation of call 1 and 2. Out of the 14 FPs of call 1, all have been labelled, but there are as per beginning of September 2010, 9 running projects plus 5 cancelled ones. Out of the 10 submitted and labelled projects of call 2, there are five projects that started, two projects have been cancelled, and three projects are still in start-up phase. Out of the five projects that started, one of them began with 2 countries involved instead of the initial 5 countries.

The quantity of POs and subsequently FPs submitted has been shrinking from call to call. This fact is not due to industry not delivering first class project ideas, as was to be seen in the "Expression of Interest," carried out for the third call CATRENE. It should be noted that in May 2008, the first call for ENIAC project proposals was launched. But with the arrival of ENIAC, the national funding budgets have not been increased and thus less funding has been allocated to the CATRENE programme. The number of POs submitted in CATRENE is 50% of the number of POs submitted in MEDEA+ phase 1 (always call 1+2+3).

Of course industry tries to avoid a significant oversubscription in calls but of course another way to overcome this issue would be to increase the countries' funding budgets.

3.3 Project Start Dates

An evaluation of Change Requests (CRs) during MEDEA+ phase 2 and CATRENE did not depict significant variances in the average number of change requests per call nor to significant variances in the grouping in minor/major CR. It however reveals that in MEDEA+ phase 2, almost all projects had the first Change Request after the actual start date of the project, whereas in CATRENE there are quite a number of projects, where the first CR was filed before the official start date of the project due to the following reasons:

- Long delay between label date and actual start date.
- Countries decide not to fund or request a reduction of resources resulting in the restructuring of the consortium and work plan.
- Different funding start dates per country require adaptation of the whole work plan.
- Changes of company-strategy of industrial partners require similar adaptations to the ones above.
- Industry cannot wait so long for implementation of projects due to time to market and finally decide to stop or to do the project outside the envisaged PPP.

Table 1a:
MEDEA+ phase 2: Project Start Date versus First CR Date (First Call)

Project		Project start date	First change request date
2A201	BLAZE	2005-01-01	2005-11-30
2A202	UPPERMOST	2005-01-01	2006-07-03
2A204	SWANS	2005-03-14	2005-12-01
2A302	ONOM@TOPIC+	2005-04-01	2006-04-26
2A401	CAR VISION	2005-04-01	2005-12-27
2A701	PARACHUTE	2005-04-01	2006-12-04
2A702	NanoTEST	2005-01-01	2005-10-20
2A703	NEVA	2005-01-01	2005-06-06
2A704	ROBIN	2005-01-01	2005-10-21
2A708	LoMoSA	2005-01-01	2006-03-06
2T101	SilOnIS	2005-01-01	2005-11-10
2T102	HYMNE	2005-02-01	2005-10-17
2T201	NEMeSyS	2005-01-01	2005-07-22
2T302	MUSCLE	2005-01-01	2005-01-20
2T304	LIQUID	2005-01-01	2005-07-11
2T401	HI-MISSION	2005-10-24	2005-06-15
MEDEA+ phase 2, call 1 projects			

White background = CR before start date.
Grey background = CR after start date.

Table 1b:
Project Start Date versus First CR Date in CATRENE

Project		Project start date	First change request date
CA101	PANAMA	2009-01-01	2009-12-18
CA103	HERTZ	2009-07-01	2009-11-02
CA301	HiDRaLoN	2009-03-01	2009-03-04
CA303	OPTIMISE	2009-07-01	2009-03-09
CA501	COMCAS	2009-03-01	2009-01-12
CT204	PASTEUR	2009-07-01	2010-02-26
CT105	3DIM3	2009-07-01	2009-04-30
CT301	EXEPT	2009-02-01	2009-03-20
CT302	TOETS	2009-03-01	2009-02-17
CATRENE call 1 projects			

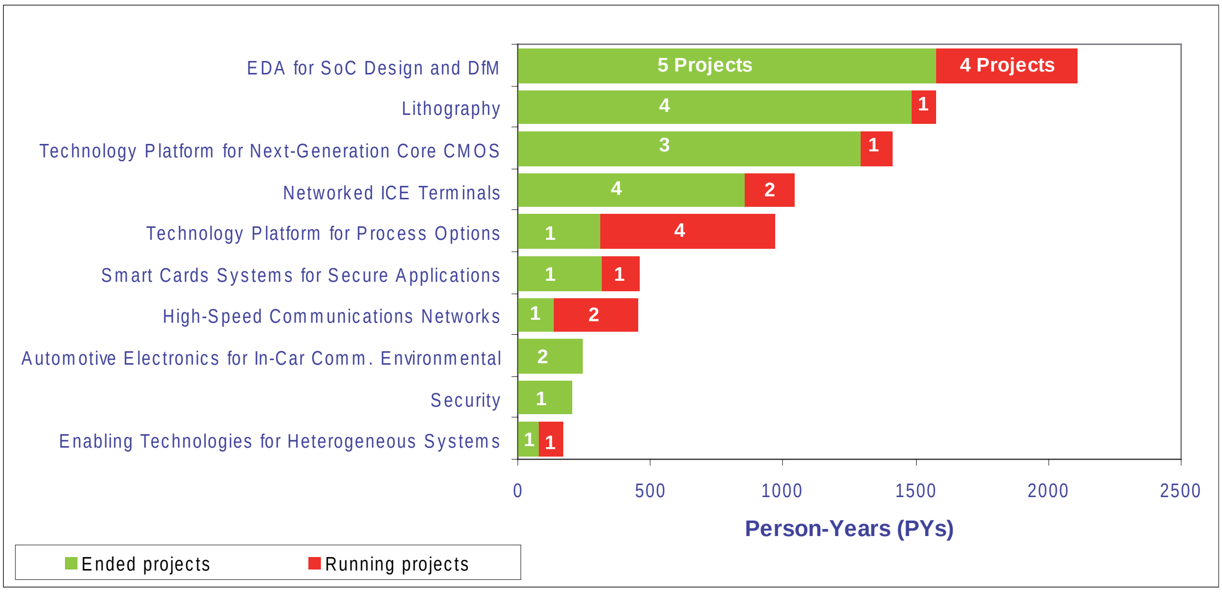
Project		Project start date	First change request date
CA104	COBRA	2010-01-01	2010-08-02
CA201	TS-CIMoNHet		
CA202	eGo	2010-07-01	
CA402	THOR		2010-01-27
CA502	SEEL		2010-01-27
CT205	REFINED	2010-01-01	2010-06-18
CT206	UTTERMOST	2010-06-01	2010-09-15
CT207	COCOA	2010-07-01	2010-09-10
CATRENE call 2 projects			

White background = CR before start date.
Grey background = CR after start date.

3.4 Projects by Work Areas

The main focus of MEDEA+ phase 2 was to develop silicon solutions for complex chips on very advanced processes with short time-to-market. Figure 3 shows in green colour the ended, in red colour the still running projects per work area as well as the person-years involved.

Figure 3:
MEDEA+ Phase 2 Resources/Projects by Work Areas (Total PYs 8,634)

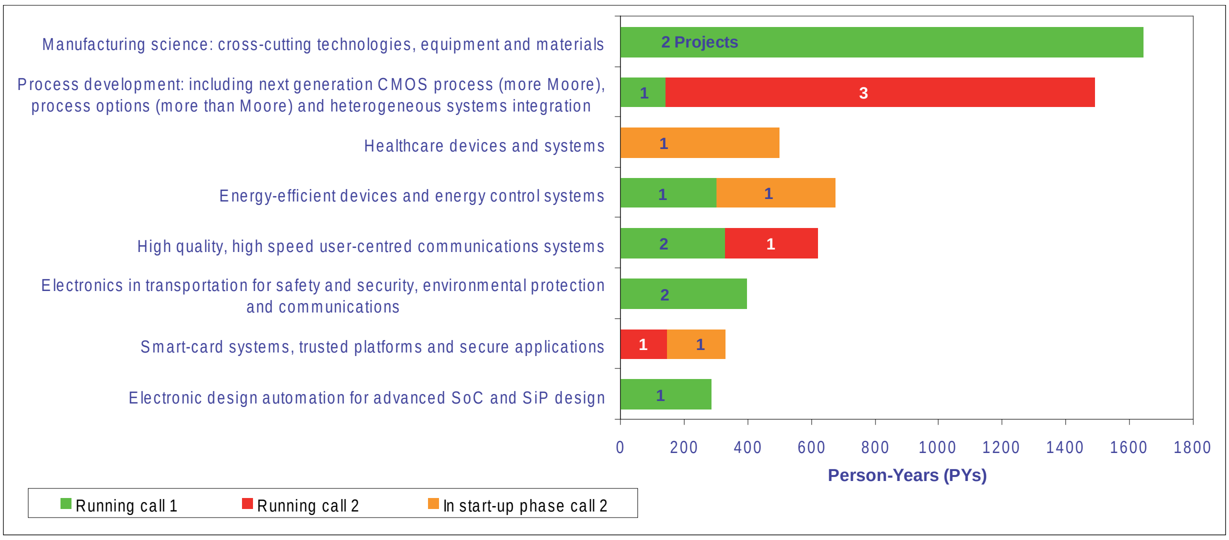


Apart from the work areas shown, one can see in figure 3 the number of projects per work area, the person-years involved as well as the differentiation in ended and running projects.

For the CATRENE programme, structured to respond to the needs of society at large and supporting the creation of lead markets, the work areas had to be redefined. Figure 4 shows the size of running and start-up phase projects for calls 1 & 2 in person-years distributed within the CATRENE work areas. Two of the 10 labelled call 2 projects have already been cancelled and it can be assumed that more changes / cancellations will come since 3 projects of call 2 are still in start-up phase and the funding of call 2 projects is not yet secured.

Call 3 projects are not part of figure 4, as they are still under evaluation.

Figure 4:
CATRENE Call 1 and 2 Resources/Projects by Work Area
(PYs 3,103 for Call 1; PYs 2,844 for Call 2)



3.5 Projects and Project's Size

MEDEA+ phase 2 projects as well as CATRENE projects are characterised by large projects, which often include a large number of partners. Figures 5 and 6 show the total projects' size in terms of person-years involved. It seems that the average project is becoming more voluminous in CATRENE; whereas in MEDEA+ phase 2, the majority of projects are in the range of 100-200 person-years, in CATRENE the majority is in the range of 200-300 PYs.

If one makes an assumption that a person-year equals € 200 000, these projects have a value between million 40 € and 60 €. It must however be noted that due to Change Requests the size of projects may alter which might have an impact on CATRENE call 2 projects.

As an average, MEDEA+ phase 2 projects have 14 partners from 4 countries, whereas the average CATRENE (referring to calls 1 & 2) projects involve 21 partners from 5 nations.

Figure 5:
MEDEA+ Phase 2 Project Size (PY)
(Ended and Running)

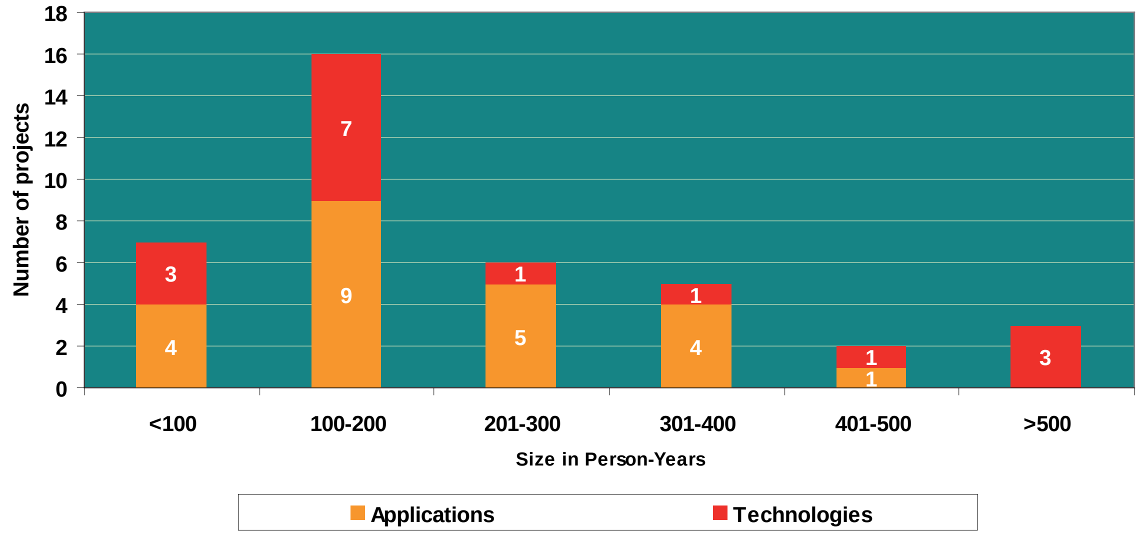
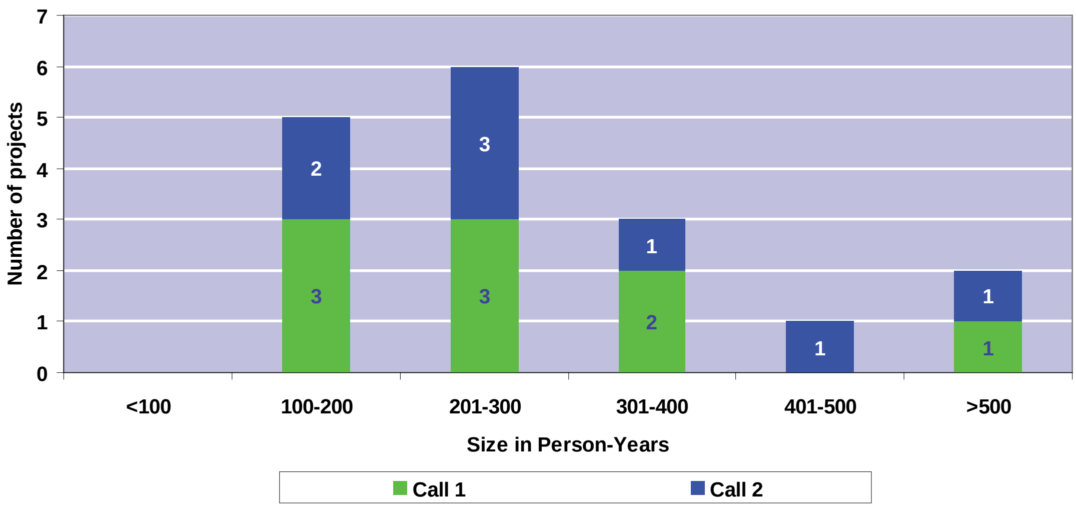


Figure 6:
CATRENE Call 1 & Call 2 Project Size (PY)
(Active Projects)



3.6 Resources and Participation

There are some quite significant changes in the structure of projects between MEDEA+ and CATRENE:

- Increasing resources of universities, a doubling from 4% to 8%
- Increasing resources of SMEs from 11% to 13%
- As a consequence, large companies are contributing less resources from 73% to 67%

Figure 7a:

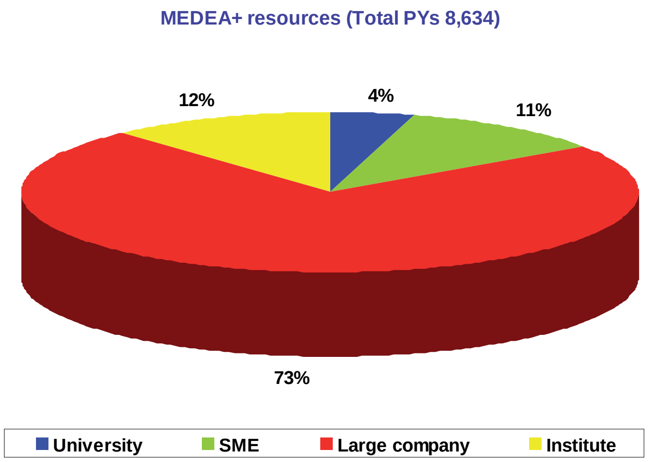
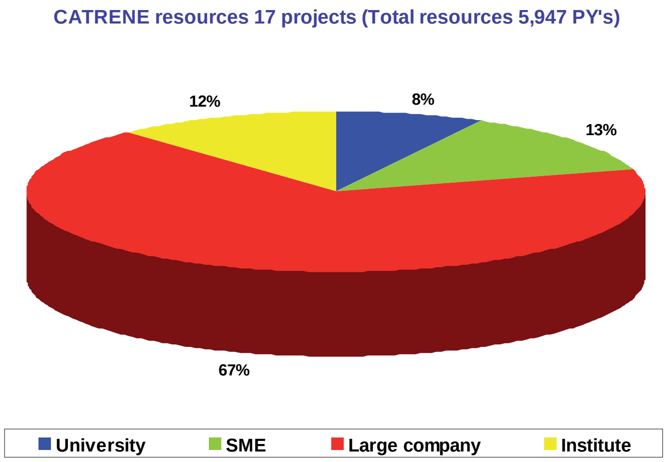


Figure 7b:



The changes in participants are in line with the ones shown above in resources.

3.7 Conferences, publishing activities, patents

The following table 2 gives a global overview on dissemination of project results. All information is delivered by industry and reported within the bi-annual Programme Reviews. Some companies however do not provide information on patents.

Table 2

PROJECTS	Publications*	PATENTS*	WORKSHOPS / EXHIBITIONS / CONFERENCES	Standardisation Activity
CA101 PANAMA	25	8	20	-
CA103 HERTZ	2	-	3	YES
CA104 COBRA	-	-	1	YES
CA301 HiDRaLoN	8	3	5	YES
CA303 OPTIMISE	19	-	12	YES
CA501 COMCAS	3	2	2	YES
2A105 SR2	35	2	29	YES
2A106 QSTREAM	39	3	17	YES
2A207 TritonZ	7	8	9	YES
2A208 iGLANCE	11	-	6	YES
2A303 BioP@SS	2	-	9	YES
2A713 HONEY	39	1	15	YES
2A714 SOFTSOC	11	-	9	YES
2A717 Beyond Dreams	11	-	18	YES
2A718 TSAR	9	-	9	-

* Both submitted and accepted

PROJECTS	PUBLICATIONS	PATENTS	WORKSHOPS / CONFERENCE CONTRIBUTIONS
2T103 - FOREMOST	108	7	61
2T104 - DECISIF	20	0	4
2T204 - ELIAS	27	0	0
2T205 – SPOT-2	5	0	6
2T206 - SIAM	18	0	15
2T210 - MaxCaps	8	0	0
2T301 - EAGLE	35	41	67
2T305 - FANTASTIC	25	4	35
2T307 - CRYSTAL	2	2	8
2T401 - HI-MISSION	14	3	44
2T405 - CoSiP	0	0	4
CT105 - 3DIM3	0	0	9
CT204 - PASTEUR	0	0	1
CT301 - EXEPT	16	3	15
CT302 - TOETS	7	4	35
TOTAL	**312**	**68**	**323**

Conclusions

The main focus of MEDEA+ Phase 2 and CATRENE was to develop equipment and silicon solutions for complex chips on very advanced processes with short time-to-market.

From the analysis of their key figures and statistics we can highlight:

- MEDEA+ and CATRENE stakeholders decided at the beginning of the programme that the average level of resources funded in labelled projects should be around 2500-3000 persons per years, the corresponding cost volume is about 500 Million Euro per year.
- The level of funding is oscillating around 120 Million Euro per year, and the 3 main supporters are the Governments of France,
- Over the years, alliances have been built, a fruitful work split of major partners of the 3 countries have led to world class eco-centres in the 3 countries applying latest state of the art technology. It might become necessary to investigate and team-up alternative co-operating partners, even outside Europe, if for whatever reasons this situation cannot be extended.
- In MEDEA+ phase 2 the majority of the project size is between 100 and 200 person-years. In CATRENE project size is larger, with the majority in the range of 200 to 300 PYs. MEDEA+ has an average of 14 partners of 4 countries; CATRENE has an average of 21 partners and 5 countries.
- Significant changes in project structure from MEDEA+ and CATRENE are visible. Resources from Universities are doubling (from 4% to 8%), contributions from SMEs have increased (from 11% to 13%). Consequently, large companies' contribution has declined (from 73% to 67%). Nevertheless, founding members belonging to large companies continue to play an important role across all areas and projects even though, total resources from them have shrunk.
- Dissemination of know how by publications, workshop/conference contributions and patents continues to remain relevant.

4. MEDEA+ PHASE 2 & CATRENE MAIN PROGRAMME ACHIEVEMENTS

4.1 MEDEA+ VISION

The vision of the MEDEA+ programme for Europe was to become a leader in system innovation on silicon, thus accelerating Europe's transformation into an Information Society.

A clear strategy was derived from the vision: if Europe is to positively influence its technical, economic and social future, ICT and their enabler microelectronics must be strong in Europe.

Moreover, the 'value chain' for an Information Society can only be strong if all links are strong. The MEDEA+ programme therefore addressed the full chain from the enabling technologies (equipment and materials, design tools and methodologies, silicon processes) to applications carefully selected in due respect to their importance for the future of Europe (high speed access, smart cards and security, automotive electronics and digital consumer terminals).

The MEDEA+ programme has been targeted to maintain and reinforce wherever possible the European presence in the worldwide electronics supply chain.

Throughout the whole MEDEA+ programme this mission has been pursued, despite the increasing globalisation of the semiconductor industry, global alliances, and the internationalisation of R&D. The 'silicon' content and value of many applications - in automotive, consumer electronics, and telecommunications - is expected to grow. A lead in silicon application platforms and enabling technologies is strategically important, not only for the semi-conductor industry, but also for the European original equipment manufacturers and system houses that rely on systems innovation on silicon to maintain a lead position.

All MEDEA+ projects strictly complied with the ITRS roadmap and are leading edge applications.

MEDEA+ has been significantly contributing to achieving European leadership in areas such as lithography, consumer and automotive electronics, to providing European solutions and standards in telecom applications, and to keep pace with global developments in core silicon technologies.

4.2 CATRENE VISION

CATRENE is a four-year programme that started 01 January 2008, extendable by another four years. The cluster focuses to deliver Nanoelectronic Solutions, responding to the needs of society at large, thereby improving the economic prosperity of Europe, reinforcing industry's ability to be at the forefront of the global competition thus resulting in a Technological Leadership for a competitive European ICT industry. CATRENE is fostering the continued development of a dynamic European ecosystem with the critical mass necessary to compete at a global level in high technology industries. CATRENE is highly dynamic and flexible as needed in this field for sustaining innovation. It intends to keep the strong points of its predecessors in terms of efficiency and strong involvement of Public Authorities.

The CATRENE programme embraces all key actors in the value chain including applications, technology, materials and equipment suppliers as well as involving large companies, institutes and universities, and small and medium sized enterprises (SMEs). It is bottom up organized. The CATRENE programme addresses mostly Technologies and challenges involving a smaller number of Member States and /or partners. It focuses more on evolutionary approach; stand alone systems, improvement of existing systems and solutions, tool and technology development, equipment and material development.

The CATRENE programme aims at strengthening the competitiveness of Europe and its industry and offering innovative solutions for Europe at large. This is in line with the changing landscape of the semiconductor industry as well as the present view on technology evolution.

CATRENE is by nature a platform for finding common understanding between industrial partners and Public Authorities. It offers the needed processes for consensus and ensures the high quality of programme/ projects by continuous improvement. CATRENE is therefore the recommended tool for multi-disciplinary and multi-cluster projects. The bottom up approach and the flexibility of CATRENE is well adapted to fit all new activities/innovations coming from various scientific domains to be embedded in nanoelectronic devices or to be adapted for semiconductor activities.

4.3 Overall projects picture

The two figures 8a and 8b reflect an overall picture on the programme aspects in terms of technology:

- In figure 10b for the first time there are projects at sub-22 nm nodes
- "More than Moore" approaches require intensive R&D on all nodes except the very latest.
- Whereas in MEDEA+ phase 2 the only two pure "More Moore" projects have been in lithography (immersion and imprint), in CATRENE there are quite a number of pure "More Moore" projects.

Figure 8a:
MEDEA+ Phase 2: Technology Projects

Projects Positioning versus ITRS													
MEDEA+		Technology Node (nm)											
Project ID	Short Title	>130	130	90	65	50	45	38	32	28	22	More Moore	More than Moore
2T103	FOREMOST											X	x
2T104	DECISIF											X	X
2T204	ELIAS												X
2T205	SPOT-2												X
2T206	SIAM												X
2T210	MaxCaps											X	X
2T301	EAGLE											X	
2T305	FANTASTIC											X	
2T307	CRYSTAL											x	X
2T401	HI-MISSION												X
2T405	CoSiP												X

Legend

Focus
Development
Concept

X Mainly
x Partially

Figure 8b:
CATRENE: Technology Projects

Projects Positioning versus ITRS														
CATRENE		Technology Node (nm)												
Project ID	Short Title	>130	130	90	65	50	45	38	32	28	22	<22	More Moore	More than Moore
CT105	3DIM3													X
CT204	PASTEUR													X
CT205	REFINED												X	X
CT206	UTTERMOST												X	
CT207	COCOA												x	X
CT208	REACHING22												X	
CT209	RF2HTZ SISOC													X
CT301	EXEPT												X	
CT302	TOETS												X	X
CT304	PULSE													X
CT305	SOI 450												X	
CT306	NGC 450												X	
CT307	EYE												X	
CT308	POLL@22												X	
CT402	9D-SENSE													X

Legend

Focus
Development
Concept

X Mainly
x Partially

Call 1
Call 2
Call 3

For CATRENE, the FPs of the third call have been added to give the broadest overview.

The tables 3a and 3b reflect that application projects in MEDEA+ as well as in CATRENE are selected in a way, that they fulfil several societal needs and thus a more economical exploitation of project results.

Table 3a:
MEDEA+ Phase 2, Focus Matrix

PROJECT NAME	Communication	Transport and safety	Healthcare	Secure society	Energy saving	Digital content & entertainment	Design technology	Sensors and actuators
2A103 MIMOWA	***					*		
2A105 SR2	**				*			
2A106 QSTREAM	**					**	*	
2A201 BLAZE						**		
2A202 UPPERMOST	*					**	**	
2A204 SWANS	**	*	*	*				
2A206 ASIC-CCD	*					**	*	
2A207 TritonZ		*	*	*		**		
2A208 iGLANCE			*			**		
2A302 ONOM@TOPIC	*			***		*		
2A303 BioP@ss			*	*				
2A401 CAR VISION		***						*
2A403 Caring Cars	*	***				*		
2A502 TSC				***		*		
2A701 PARACHUTE	*	*					***	
2A702 Nano TEST							***	
2A703 NEVA						**	***	
2A704 ROBIN							***	
2A708 LoMoSA+						**	***	
2A713 HONEY							***	
2A714 SoftSoC	*					*	**	
2A717 Beyond Dreams	*						**	*
2A718 TSAR	*		*			*	**	

Table 3b:
CATRENE, Focus Matrix

PROJECT NAME	Communication	Transport and safety	Healthcare	Secure society	Energy saving	Digital content & entertainment	Design technology	Sensors and actuators
CA101 PANAMA	**				*			
CA103 HERTZ	**				*			*
CA104 COBRA	**					**	*	
CA201 TS-CIMoNHeT	*			***				
CA202 eGo	*			***				*
CA301 HiDRaLoN		*	*			*		**
CA303 OPTIMISE		**			*	**		
CA402 THOR		*	*		*		*	
CA501 COMCAS	**				**		*	
CA502 SEEL		**			***			

Nightingale was cancelled in 06/2010.

*, **, *** Ascending level of implication

4.4 Summary of sustainable MEDEA+ and CATRENE programme successes:

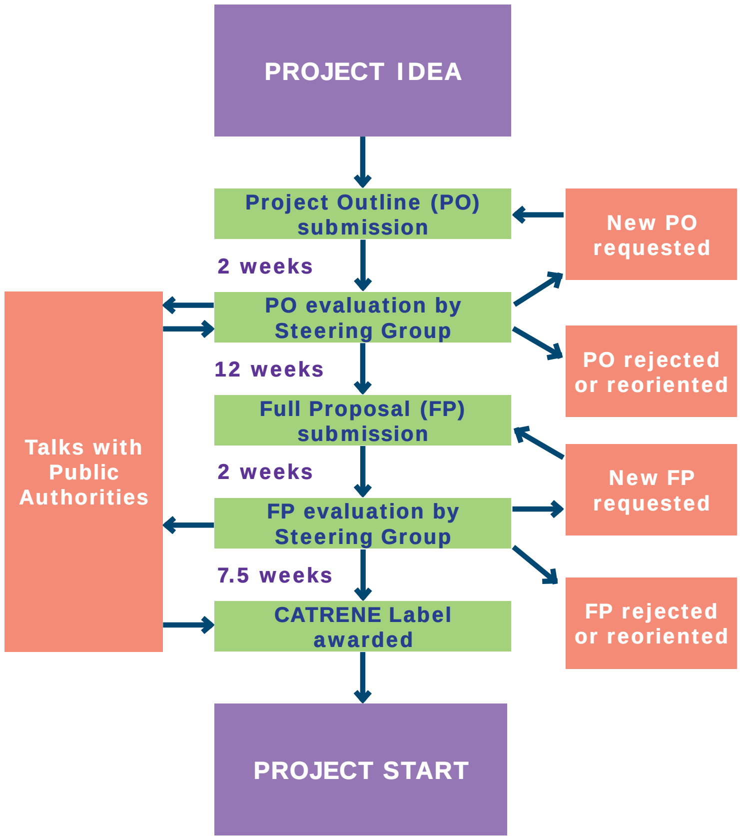
An efficient project management and monitoring process is contributing substantially to the success of MEDEA+ and CATRENE. The experience accumulated by JESSI, MEDEA and MEDEA+ has resulted in a set-up of multiple interaction processes to allow updates on Project Outlines (PO) and Full Proposals (FP) taking into account the comments given by Public Authorities and CATRENE experts.

The main criteria for project selection are the following:

- Commitment to CATRENE vision and objectives
- Innovation in basic and industrial research
- Existing European R&D capacity
- Competences of the partners
- Strengths of the consortium ("team effect")
- World market potential
- Leverage effect on employment
- Meeting societal needs
- Positive funding outlook and matching of eligibility criteria of MS

CATRENE organises an annual call for proposals, see following table.

Table 4:
CATRENE Call Evaluation Process



The selection of projects follows a four step evaluation taking into account the possibility to update Project Outline (PO) and Full Proposal (FP)

The **Project Outline (PO)** is providing a brief overview of the project's objectives and the partners in the consortium. It allows early advice and feedback from the CATRENE Steering Group to the proposers and preliminary discussions with the public authorities.

Pending approval of the PO by the CATRENE Steering Group, projects are invited to submit a **Full Proposal (FP)**. The FP is an update of the PO document in which particularly the project organisation, schedule and tasks with list of deliveries are detailed. In addition this document must answer to comments and recommendations delivered both by CATRENE and Public Authorities during the PO phase. The process of improvement is applied also for the FP stage, conducting in a real value added for the consortium and guarantees a better chance of success for the project. On the strength of this document and the willingness of the relevant Public Authority to fund, the CATRENE label may be awarded.

The role of the Steering Groups has to be highlighted in this continuous montoring process. The Steering Groups members are experts from industry active in the same domains as covered in the projects in question, but not involved in those projects.

MEDEA+ and CATRENE are eager to maintain the same experts from the proposal selection phase till the end of the project. All experts' reviews are shared within the Group first in order to consolidate expert evaluations and second to detect potential biased evaluations.

The project label is proposed by the Steering Groups and awarded by the Support Group.

A technical report is requested twice a year and an on-site review is managed every year. The reports are reviewed by the Steering Groups. Such a review may generate requests for more information

or corrective actions. These reports are mandatory to follow the project progress and detect any deviation from the original plan.
Technical issues, consortium reorganisation following a partner participation reduction or withdrawal (funding issue or re-orientation of partner R&D strategy priorities…) are among the most common source of project re-orientations.

In order to update the project plan, such re-orientations are described in a Change Request (CR), which is an amended version of the original proposal.

The Change Requests are also reviewed by the Steering Group. They decide if an amended project remains of interest in line with the main criteria for the project selection. The result may lead to the Change Request approval, a request for modification and in the worst case label-withdrawal.

As a matter of fact, the management of Change Requests is a rather important activity, leading to high quality levels of project results.

Following is a list of major MEDEA+/CATRENE programme successes:

- Breakthroughs in wireless broadband (low-cost version, convergence fixed/wireless) and multimedia systems and terminals. (2A103-MiMoWA, 2A105-SR2, 2A106-Qstream, CA101-PANAMA, CA103-HERTZ, CA2A201-BLAZE, 2A202-UPPERMOST, 2A207-TritonZ)
- In automotive electronics, essential contributions to platform development, substantial achievements in reliability, safety and intelligent features for vehicles. (2A401-Car Vision, 2A403-Caring Cars, 2T204 – ELIAS, 2T205 – SPOT2)
- European smart card and security activities have created standards and technologies as enablers for new applications, dominating the global smart card market. (2A302 Onom@Topic, 2A303-BioP@ss, 2A502-TSC, CA201-TS-CIMoNHet, CA202-eGo)
- European leadership in Lithography with worldwide market-share >70%. (2CT301 - EAGLE, 2T304 – LIQUID, CT 301 – EXEPT)
- Innovations at material and substrate levels boosting device performance and strengthening European competitiveness. European leadership in SOI with world wide market share >70%. The European developments of new ultra high dielectric (UHK) materials as well as ALD (Atomic Layer Deposition) techniques are largely used world wide for future technology nodes. (2T101 – SilOnIS, 2T104 – DECISIF, 2T210 – MaxCaps)
- Establishment of a silicon technology platform for emerging high frequency RF and mm-wave. (2T206 – SIAM, 2T401 – Hi MISSION)
- Fully integrated technology platforms for embedded Non Volatile Memory. (2T405 – NEMeSYS, CT205 REFINED)
- Mature 3D integration technology platforms and innovative packaging SiP. (2T405 – CoSiP, CT207 – COCOA, CT105 – 3DIM3)
- Europe is on a par with global competition in advanced basic CMOS process developments (100 nm to 45 nm). One European company has been amongst the first manufacturers in the world to offer a 45 nm Low Power technology. (2T103 – FOREMOST, CT206 – UTTERMOST)
- Europe is leading in EDA and design technology innovation. (2A701- PARACHUTE, 2A702-NanoTEST, 2A703-NEVA, 2A704-ROBIN, 2A708-LoMoSA+, 2A713-HONEY, 2A714-SoftSoC, 2A717-Beyond Dreams, 2A718-TSAR, CA303-OPTIMISE, CA104-COBRA, CA501-COMCAS).

4.5 SMEs, a Growing Partner Group

Whereas the number of participating SMEs in MEDEA+ phase 2 increased slightly towards the end of the programme, a change in the SME policy of some member states pushed participation as well as contributing resources from 2009 onwards. The impact on CATRENE can be seen in figures 9 and 10. It has already been stated in section 3.7 that the SME resources between MEDEA+ phase 2 and CATRENE went up from 11% to 13%. With 35% participation and 39% contribution of involved SME resources, the French SMEs are the champions in this partner group. In the CATRENE projects it becomes visible that The Netherlands are now pushing SMEs towards more involvement: from 10% participation in MEDEA+ phase 2 to 23% in CATRENE call 1 & 2 as shown in figure 11.

Figure 9:
SME Participation per Year

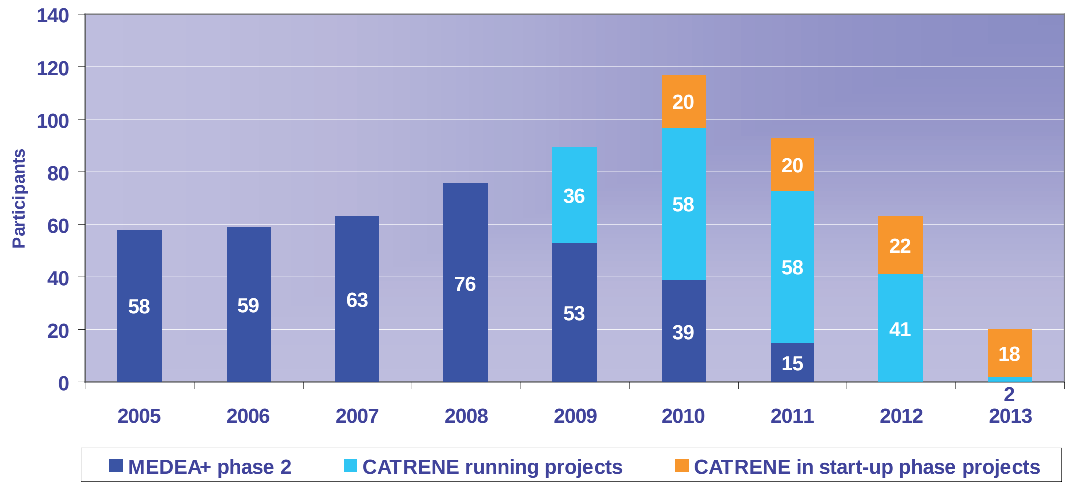


Figure 10:
SME Resources per Year

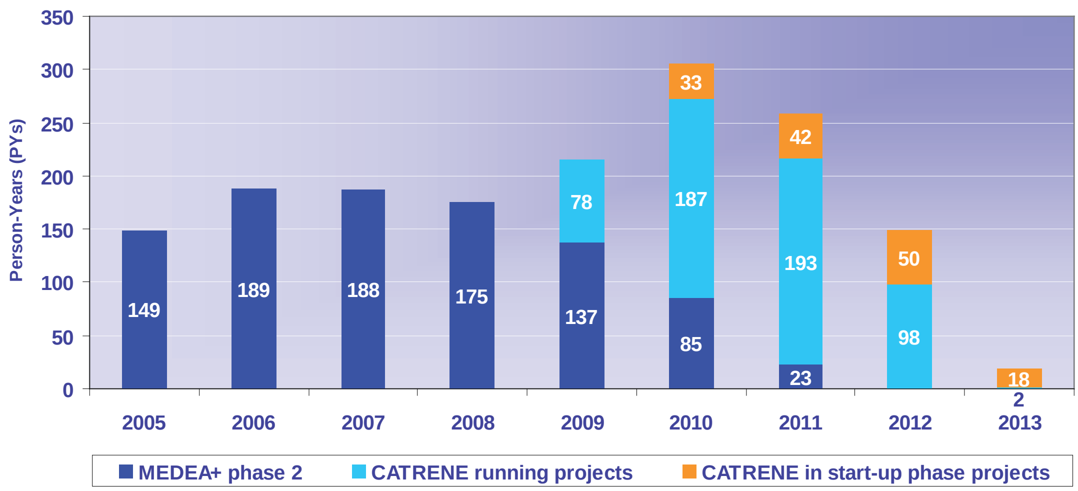
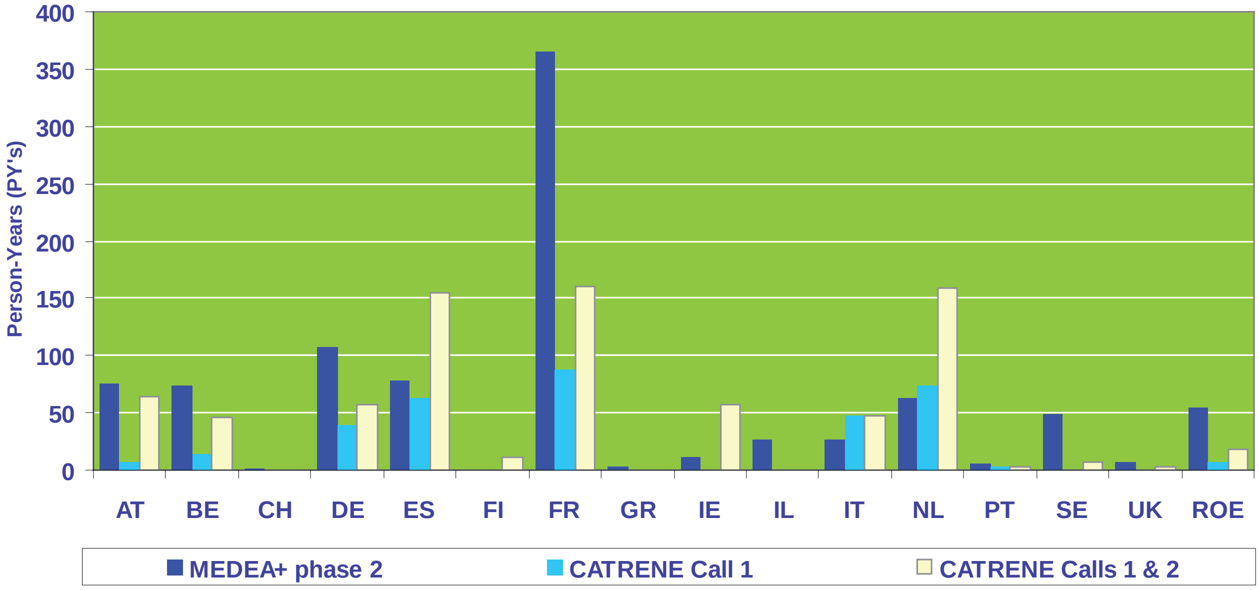


Figure 11:
SMEs by Countries



As can be seen in figure 12, two MEDEA+ phase 2 work areas have attracted the most SMEs: EDA with 24% and Technology Platform for Next Generation Core CMOS with 18%. As a matter of fact, EDA activities have always been a strong domain for SMEs.

Figure 12:
SMEs in MEDEA+ Phase 2 by Work Area
(% of SME – PYs)

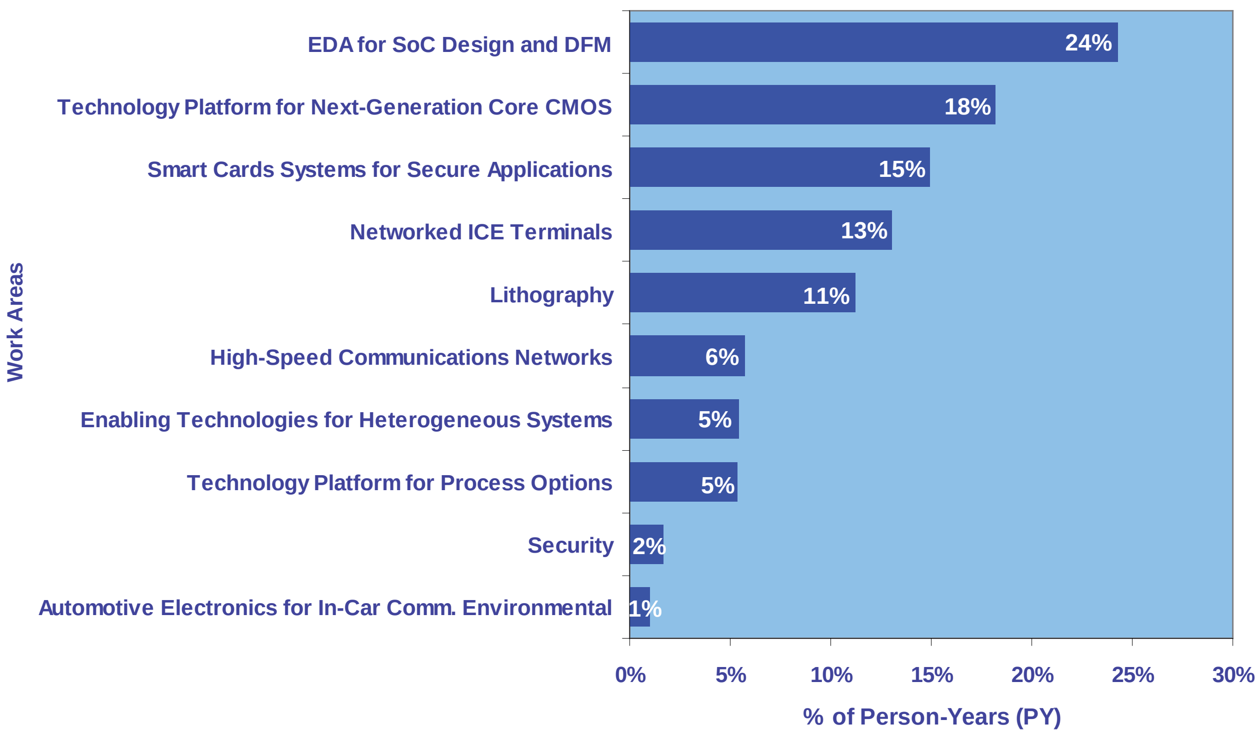
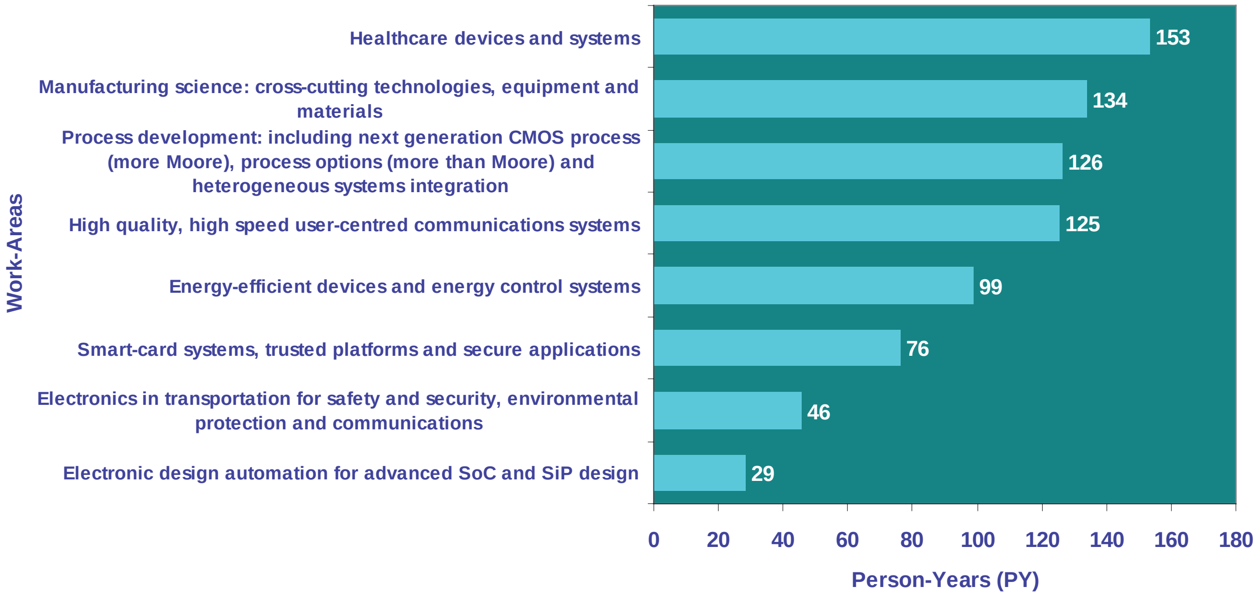


Figure 13:
SMEs in CATRENE Calls 1 & 2 by Work Area
(SME – PYs)



A new SME group has been attracted into the frame of CATRENE, these being ones active in healthcare devices and systems.

4.6 EDA Roadmap and Design Technology Conference (DTC)

Investment in EDA is crucial to the future of the European micro- and nanoelectronics industry. For a long time, design automation resources have lacked engineering and performance maturity, resulting in a bottleneck and thus endangering Europe to fully exploit all possibilities of current and future silicon processes. All EUREKA programmes in micro- and nanoelectronics have therefore focused on developing knowledge and expertise in design automation.

In 2005, the MEDEA+ EDA Roadmap was released. In January 2009, the follower of the MEDEA+ roadmap, the European Design Automation Roadmap was issued. This edition mainly focused on demonstrating a complete top-down design flow, starting at specifications, then System Level Design linking designers to formal customer's specifications, parametrisable IPs creation, standards and Design for Manufacturability (DfM) supported by new TCAD (Technology CAD) developments.

The EDA roadmap activities are part of the overall effort of MEDEA+/CATRENE to reach adequate design efficiency and maturity for all the design steps between system level specification and signal integrity solutions, enabling especially SMEs to work closely together with large industry but also with academia. The EDA roadmap is well recognized on international level by the experts' community as a unique and useful document. It has resulted in a favourable environment for EDA SMEs development.

At the yearly held Design Technology Conferences, application-oriented design technology for micro- and nanoelectronics have become a prominent theme for experts from European system, design and semiconductor companies presenting latest project results and exciting highlights from MEDEA+/CATRENE projects. The conference is always held in conjunction with a national PdC (Pôle de Competitivity).

4.7 European Nanoelectronics Forum and Quotes

The annually held MEDEA+ Forum has been since 2008 a common event organized by CATRENE, the EUREKA cluster programme, and the ENIAC Joint Undertaking, both public-private partnerships working in close synergy for European leadership in nanoelectronics. It is for all MEDEA+/CATRENE and ENIAC JU stake holders an excellent opportunity to have an update on Europe's major R&D co-operative programmes and projects. The forum is a two day event consisting of a plenary session with prestigious keynote speakers from industry, public authorities and academia. As well, there is a panel session and a press conference. In addition, there are time slots dedicated to poster and demo sessions where project consortia present their goals/activities and results. The poster and demo session is highly appreciated by all participants due to its intensive networking possibilities.

Some details about the forum:

- Around 250 – 300 participants
- 500m² area for poster and demo sessions
- Prominent Guest and Keynote speakers from industry and politics presenting opinions on most recent hot topics
- Forum press conference and press lunch
- Forum dinner with the award of the most innovative project

Around the main event, there are major additional meetings with various MEDEA+/CATRENE and ENIAC JU bodies. The Forums have taken place at:

2001: Amsterdam
2002: Antwerp
2003: Berlin
2004: Paris
2005: Barcelona
2006: Monte Carlo
2007: Budapest
2008: Paris
2009: Noordwijk
2010: Madrid

Figure 14:
Forum Dedicated Web Pages

During the forum, there is the award for the most innovative project of the year, the Jean-Pierre Noblanc Award. Already in the forefront there are stringent selection criteria for projects starting in the labelling phase. The benefits are projects with an excellent quality. Of course there are additional selection criteria for the winner of this award.

The main criteria are:

- Innovation level of project results,
- Exploitation potential,
- Anticipated market impacts,
- Specific impacts on European economy,
- Quality and efficiency of project,
- Co-operation and management,
- Effectiveness of resource spending.

Table 5:
Jean-Pierre Noblanc Award History

Year	WINNER PEOJECT NAME	WINNER PROJECT CODE
2004	CMOS Logic 0.1 aem	T201
2005	Pocket-MM	A207
2006	PICS	A406
2007 (Two winners)	Onom@Topic Silonis	2A302 2T101
2008	BLAZE	2A201
2009	ELIAS	2T204

Quote from the French MDC at the occasion of opening the European Nanoelectronics Forum 2008:

"Eureka clusters have indeed proved to be **very efficient tool**s to foster the cooperation between European players: they were in fact deeply **needed to remain in the fierce race** we have to face in nanoelectronics.

And what are the results of these almost 20 years of cooperation? Let me **name 3 of them**:

- **Firstly, several European semiconductor companies** are now **among the very first** on their market;
- **Secondly, two European equipment-material suppliers** have **emerged as world leaders** in their respective market;
- **And thirdly, we have given access** to the most advanced nanoelectronics technologies **for European electronic systems providers** in fields such as telecommunications, aeronautics, automotive, defence or industrial electronics.

And most important, EUREKA clusters, such as MEDEA+, have enabled European players to **work together and create critical masses** by **linking the major European clusters**, already long before "pôles de compétitivité" where officially labelled by Governments."

Quote from the Dutch Minister of Economic Affaires at the occasion of opening the European Nanoelectronics Forum 2009:
"Europe has always been an important global player in this sector. Knowledge, innovativeness and research have always been European strengths. And they still are! Companies like STMicroelectronics, Infineon, ASML, Philips - to name just a few - and institutions like IMEC in Belgium, Fraunhofer in Germany and CEA-LETI in France **are players of world-class calibre**.

But their position is far from uncontested. Over the last decades we have seen the emergence of new strong actors, mainly in Asia. Companies that are extremely efficient and can benefit from economies of scale, an abundance of highly skilled young people, attractive wage levels and – last but not least - substantial public incentives.

These are formidable competitors for the European industry. But it is a battle we have to face, if Europe wants to maintain its position on global playing field.

It is my firm conviction that Europe is able to maintain a leading role as innovator and entrepreneur in nanoelectronics, as long as we are prepared to make better use of the vast resources of expertise available on this continent.

Cooperation is the key word here! And cooperation need not conflict with national policy objectives. Far from it!

Programmes like CATRENE and ITEA2 have profoundly changed the way European companies and institutes work together and share precious resources. They have offered the European industry a real competitive advantage, globally speaking. I think it is fair to say that the JTIs have been based upon this successful concept."

Communiqué: The EUREKA Ministerial Conference
XXV Session
Berlin, 25 June 2010

Point 8:

The Ministerial Conference welcomed in particular the establishment of a new **EUREKA Innovation Award** as a means of better visibility of EUREKA and as incentive for project participants. It congratulated this year's winner project ONOM@TOPIC+ for its outstanding achievements in developing a European smartcard platform for citizenship and mobile multimedia applications that makes life easier and more secure for users while adding value for network operators.

ONOM@TOPIC has been number 1 winner of the EUREKA Innovation Award 2010. And MEDEA+ project FOREMOST is sharing together with another EUREKA project the number two position.

GERMANY 2009 2010 EUREKA CHAIRMANSHIP

German EUREKA Chairmanship 2009 | 2010

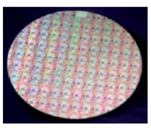
EUREKA Innovation Award 2010

THE PROJECTS

E!417 EUROMAR MERMAID (1988-1998)

Participating countries: Germany, Norway, Canada

Measuring agricultural nutrients and industrial wastes that pollute Europe's coastal waters has mainly been performed by ship-b consequently irregular process, prone to underestimating real levels of pollution. MERMAID's solution is a system of automated, locations in coastal waters that communicate with shore stations in a bi-directional way. Download a movie clip



MEDEA+ 2T103 FOREMOST (2006-2008)

Participating countries: France, Belgium, Germany, Greece, Israel, Italy, Netherlands, United Kingdom

Complementary metal oxide semiconductor (CMOS) technology based on silicon wafers dominates chip manufacture. To maintain Europ FOREMOST has developed advanced process modules and transistor architectures and demonstrated a full CMOS 45nm process technolo facilities. Download a movie clip

MEDEA+ 2A302 ONOM@TOPIC+ (2005-2007)

Participating countries: France, Czech Republic, Hungary, Netherlands, Spain, Sweden

ONOM@TOPIC+ has developed a European smartcard platform for citizenship and mobile multimedia applications that makes life easi network operators. It is used by European governments to issue interoperable documents (citizen card, visas or passport documen access to e-Services. Download a movie clip

BMBF-Pressemitteilung vom 25. Juni 2010, Seite 1
(only available in German language)

Bundesministerium für Bildung und Forschung

Freiheit Einheit Demokratie

Presse-mitteilung

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25. Juni 2010

Schütte: „Spitzeninnovation dank internationaler Kooperation"

Staatssekretär überreicht in Berlin erstmals EUREKA Innovation Award

Staatssekretär Georg Schütte hat am Donnerstagabend in Berlin den EUREKA Innovation Award 2010 verliehen. Gewinner des erstmals vergebenen Preises ist ein Projekt des EUREKA-Clusters MEDEA+, das in der Mikro- und Nanoelektronik für herausragende technische Innovationen steht und somit Europas hohen Stellenwert in diesem weltweit bedeutenden Industriezweig sichert. „Wir haben das Leitmotiv unserer Präsidentschaft auch zum Thema des diesjährigen EUREKA Innovation Award 2010 gemacht", sagte Staatssekretär Schütte. Spitzeninnovation durch internationale Kooperation, so laute dieses Motiv. „Mit diesem Preis sollen Innovationen ausgezeichnet werden, die aufgrund internationaler Kooperationen entwickelt wurden oder die auf internationalen Märkten besonders erfolgreich vermarktet werden konnten." Das zu ermöglichen, dafür werde EUREKA auch künftig stehen, so Schütte.

Das Gewinner-Projekt „MEDEA+ 2A302 ONOM@TOPIC+" unter der Leitung der französischen Firma Gemalto hat eine europäische Smartcard-Plattform für amtliche Identitätsdokumente und mobile Multimedia-Anwendungen entwickelt. Genutzt werden diese Technologien insbesondere von europäischen Regierungen beim Ausstellen von Ausweisdokumenten. Die darin eingebauten Speicherchips eröffnen den Nutzern von mobilen Endgeräten oder Smartcards eine große Bandbreite an elektronischen Diensten – von mobilen Bezahlsystemen über sichere Identifizierung bei Bankgeschäften bis hin zum Zugang zu digitalen Informationen zu jeder Zeit und an jedem Ort. Insbesondere Smartcard-Projekte sind für Europa von großer Bedeutung, da die europäische Industrie hier führend in der Entwicklung und Fertigung ist.

Conclusions

- An efficient project management and monitoring process is contributing substantially to the success of MEDEA+ and CATRENE. the management of Change Requests is a rather important activity, leading to high quality levels of project results.
- Major break-through in MEDEA+ and CATRENE include wireless broadband and multimedia systems and terminals, automotive electronics with essential contributions in reliability, safety and intelligent features for vehicles; in smart card and security standards and technologies for new applications on top of dominant position in global markets; in equipment and materials leading worldwide position in lithography and in SOI, in ultra high dielectric (UHK) materials as well as ALD (Atomic Layer Deposition) techniques. MEDEA+ and now CATRENE reinforce industry's ability to be at the forefront of the global competition and responding positively to the need of European society at large, thus improving the economic prosperity of Europe.
- Whereas the number of participating SMEs in MEDEA+ phase 2 increased slightly towards the end of the programme, a change in SME policy of some member states pushed participation as well as contributing resources from 2009 onwards. French SMEs continue to be champions in this partners group but The Netherlands is pushing hardly now for SMEs involvements.
- The first EDA roadmap was released by MEDEA+ in 2005 and a new one followed produced by CATRENE in 2009. The EDA roadmap is part of the overall effort to reach adequate design efficiency and maturity for all design steps between system level specification and signal integrity solutions. The EDA roadmap is well recognized by the experts' community as a unique and useful document.
- The annually held MEDEA+ forum became in 2008 a common event organized by CATRENE and ENIAC allowing all stake holders to have a joint update on Europe's major R&D co-operative programmes and projects to discuss on common strategic objectives and to build network.

5. INSIGHTS FROM MAIN EUROPEAN R&D ACTORS

In this subchapter, some insights from company interviews are given; these interviews, done by independent consultants[1], have been held end of 2008, when carrying out the study "Impact of Micro/Nanoelectronics on the European economy."

European Individual Device Manufacturers (IDMs): IDMs have today the means to adapt to the changing global landscape. What is currently at stake is their capacity to generate wealth in and for Europe.

European IDMs cannot be competitive against Asia in advanced CMOS manufacturing activities without similar incentives and economical environment but remain committed to More than Moore and derivatives manufacturing in Europe. Complex integration and application-driven system design is recognized to be at the heart of the European semiconductor industry added value and correspond to European market requirement.

European IDMs will continue to maintain their design activities in Europe for mainly 4 reasons:

- quality of R&D and skilled engineers,
- relationship with European OEMs and world class labs in comprehensive ecosystems (automotive, telecoms, security, etc.)
- cumulated knowledge based on 30 years of continuous semiconductor design activities in Europe
- heterogeneous manufacturing base making possible to maintain the required interaction between design and technologies in existing and emerging markets

However, European IDMs acknowledge the fact that the long-term competitiveness of design activities in Europe is dependent upon the critical size of the European semiconductor industry. An adequate level of public support is therefore mandatory in order to balance the global level playing field and maintain the required level of manufacturing, including in advanced CMOS process, to support design activities.

In addition, a future shortage of skilled people should be anticipated. Although European engineers have good skills and know-how, China produces more engineers than Europe and the US together and, Asian countries are committed to develop their design expertise and start to build their cumulated knowledge.

They point out that IP protection and standards should be used in order to both secure the European technological leadership areas and maximize the benefits of the European market size through common policies.

For them, cooperative R&D programmes are key instruments to the long-term attractiveness of Europe in design activities, by ensuring the critical size of projects and maintaining the collaborations between companies working in Europe for Europe.

In order to raise economic growth, most of the European countries are presently checking whether or not to expand or shift their mix of policy tools, such as incentives or tax privileges.

It should however be noted that clusters like CATRENE generate additional value and benefits over the mere financial incentives or tax privileges: increased efficiency by vertical cooperation. The capability and efficiency of teamed-up partners is much higher than the aggregation of individual partner capabilities, but without PA's seed this booster cannot be accomplished.

Equipment and material suppliers: These suppliers to the semiconductor industry have to maintain close connections with market leaders in order to develop their technological leadership. European companies

[1] Cabinet Decision

maintain a strong presence in Europe thanks to their localization in R&D clusters, which facilitates collaborations with world-class academia, research labs and IDMs.

European equipment and material suppliers have strongly benefited from cooperative R&D programmes in order to build their world leadership positions. Reference is made to lithography equipment and SOI material. Today the global competitiveness of E&M companies in selected areas generates added value for Europe by participation in the global food chain of microelectronics and not only by supporting the European semiconductor companies. With appropriate funding there is a good chance that the European E&M companies can further improve their global positioning and that they are able to extend their activities also to other areas. As the E&M market strongly reacts to the industry cycles, funding is important to reduce the impact and maintain the R&D intensity in downturn periods.

Research labs: Academia and research labs are key assets of the European semiconductor industry and attract the best talent and leaders worldwide, supporting the attractiveness of Europe for R&D activities.

Recognizing the quality of the technological and application scopes of European collaborative R&D programmes, they all insist on the fact that Europe has to be careful not to loose contact with More Moore technologies in order to maintain its long-term competitiveness and innovation power in More than Moore.

They also acknowledge that cooperative R&D is a must in order to stimulate collaborations within the value chain that are required by new emerging markets including societal needs.

Their business models may differ depending on their localization, some being driven by local industrial collaborations while others are mainly working with international partners. However and since the competitive landscape is global, their opinion is that European funding should be concentrated on the best of class players and driven by a European industry policy with a clear objective to increase the competitiveness of European players against other regions.

OEMs and service providers: Depending on the technological intensity in their respective application markets, OEMs and service providers have not all the same proximity with semiconductor technologies. However, they all confirm the fundamental role of semiconductor technologies in their global competitiveness and technological independence.

Technological rupture requires close collaboration between OEMs and technology providers. Maintaining the access to the semiconductor technology thus remains key to stimulate the economy and consolidate employment in Europe through innovation.

In new application fields such as medical or retail as well as in existing applications, system approach is mandatory in order to justify the investment and not simply add solutions on existing infrastructures with limited benefits. OEMs and service providers are more and more looking for complete solutions from semiconductor suppliers, including embedded software and its ecosystem. For OEMs, it is not the proximity with manufacturing but the proximity with design that is important. They are more concerned by the capability of one semiconductor supplier to master the integration of several technologies than by the localization of manufacturing.

OEMs and service providers all agree on the fact that technology standardization and regulations are mandatory in order to facilitate market development. They believe that Europe could seize the opportunities of emerging societal needs to build world leaderships, which is requiring a European vision and strategy backed by a proactive support of PAs to the food chain.

Conclusions

- Public support is mandatory in order to balance the global level playing field and maintain the required level of manufacturing, including in advanced CMOS process, to support design activities. Especially for vertical cooperation in R&D, public support is the seed for creating the consortia of European champions.
- Cooperative R&D programmes are key instruments to the long-term attractiveness of Europe, by ensuring the critical size of projects and maintaining the collaboration between companies working in Europe for Europe.
- European IDMs cannot be competitive against Asia in advanced CMOS manufacturing activities without similar incentives and economical environment but remain committed to More than Moore and derivatives manufacturing in Europe.
- European equipment and material suppliers have strongly benefited from cooperative R&D programmes in order to build their world leadership positions. Today the global competitiveness of E&M companies in selected areas generates added value for Europe by participation in the global food chain of microelectronics and not only by supporting the European semiconductor companies.

6. FINAL CONCLUSIONS

- MEDEA+ ensured Europe's competitiveness in semiconductor technology, delivered essential breakthroughs and thus decisive European domains in numerous applications and systems, brought leadership in lithography on a worldwide scale and boosted Europe's contribution in materials and substrates.
- The number of participating SMEs in CATRENE versus MEDEA+ phase 2 is increasing. This is in accordance with some country' policy, e.g. France and The Netherlands.
- CATRENE is the recommended tool for future multi-disciplinary and multi-cluster projects. The bottom up approach and the flexibility of CATRENE is well adapted to fit all new activities/innovations issued from various scientific domains to be embedded in nanoelectronics devices or to be adapted for semiconductor activities. The Joint Technology Initiative (JTI) ENIAC launched by EU and Member States cannot replace the EUREKA bottom up approach of CATRENE. The ENIAC, top down approach, reflects priorities at the European level for the benefit of a large number of European countries. The ENIAC projects should be dedicated to addressing the "Grand Challenges" for Europe. Based on the concept of flexibility and in its open mind set, CATRENE is adapted to major technology breakthroughs and not restricted to the Grand Challenges only.
- Cooperative R&D programmes are key instruments to the long-term attractiveness and competitiveness of Europe's semiconductors' capability ensuring the critical size of projects and maintaining the collaboration between companies working in Europe for Europe.
- Nothing is so persistent as the race for "Innovation." Europe cannot stop to manage the challenges of societal needs. Europe has to deliver the required innovations. Europe has to master the latest technological evolutions in nanoelectronics in order to shape its future on time and defend its economical independence.
- **Europe needs the continuation of the precompetitive research in nanoelectronics within the CATRENE cluster programme beyond 2011.**

ANNEX A: MEDEA+ & CATRENE PROJECTS

For the evaluation in this section the below shown set of 39 MEDEA+ phase 2 and 17 CATRENE projects are providing the basis.

List of projects (September 2010)

MEDEA+ phase 2 projects		CATRENE projects
ENDED	RUNNING	CALL 1
2T101 SilOnIS	2T104 DECISIF	CT105 3DIM3
2T102 HYMNE	2T204 ELIAS	CT204 PASTEUR
2T103 FOREMOST	2T205 SPOT-2	CT301 EXEPT
2T201 NEMeSyS	2T206 SIAM	CT302 TOETS
2T301 EAGLE	2T210 Max Caps	CA101 PANAMA
2T302 MUSCLE	2T307 CRYSTAL	CA103 HERTZ
2T304 LIQUID	2T405 CoSiP	CA301 HiDRaLoN
2T305 FANTASTIC	2A207 TritonZ	CA303 OPTIMISE
2T401 HI-MISSION	2A713 HONEY	CA501 COMCAS
2A103 MIMOWA	2A105 SR2	CALL 2
2A201 BLAZE	2A106 Qstream	CT205 REFINED
2A202 UPPERMOST	2A208 iGLANCE	CT206 UTTERMOST
2A204 SWANS	2A303 BioP@ss	CT207 COCOA
2A206 ASIC-CCD	2A714 SoftSoC	CA104 COBRA
2A302 ONOM@TOPIC	2A717 Beyond Dreams	CA201 TS-CIMoNHet
2A401 CAR VISION	2A718 TSAR	CA202 eGo
2A403 Caring Cars		CA402 THOR
2A502 TSC		CA502 SEEL
2A701 PARACHUTE		
2A702 Nano TEST		
2A703 NEVA		
2A704 ROBIN		
2A708 LoMoSA+		
# 23	# 16	# 9 + # 8

1. MEDEA+ PROJECTS IN TECHNOLOGIES

2T101: SiLOnIS

Objective:

The overall objective of this project is to provide within 3 years an industrial source of large diameter strained SOI. The project aims at building a strained SOI technological platform gathering the main European actors in substrates, metrology and ICs in order to fasten the development of high mobility (strained) SOI wafers and to shorten their introduction in a IC fab environment. The radical change for this new generation of smart substrates development is that the strain brought by substrates is independent on the technologic flow. So the substrate platform encompasses the processing compatibility of these new substrates with sub 65nm technology in the industrial environment of ICs makers. High mobility “strained Si” and “SOI” are two breakthroughs that the consortium wishes to combine in one single technology platform for high performance ICs.

Project members:

2T101/C SiIOnIS		
ENDED	AIXTRON	DE
	AMD SAXONY	DE
	ASM FRANCE	FR
	FREESCALE CROLLES	FR
	JOBIN YVON	FR
	LETI	FR
	NANOMETRICS	UK
	NXP SC	FR
	OMI	IE
	SILTRONIC	DE
	SOITEC	FR
	SOPRA	FR
	STMICROELECTRONICS	FR

Dates and Resources:

This project began as planned in January 1st 2005 and ended in December 31st 2007.

The original project lifetime on 36 months was met.

Total manpower: 199.5 P.Y.

Status and Achievements:

An industrial source of large diameter substrates (200mm and 300mm) combining high mobility strained Si and SOI was provided as an alternative to local strain approaches. Theses wafers have been developed and carrier mobility based on two generations Germanium concentration has been investigated. Devices based on both generations have been designed, manufactured and successfully characterized. This project has contributed to improve speed performances of electronic devices and reinforce the technogical advantage of European semiconductor industry.

The SiLOnIS project won the Jean Pierre Noblanc for Excellence Award in 2007.

2T102: HYMNE

Objective:

The HYMNE project aims at developing methods, software and hardware that enable the European IC manufacturing industry to enhance production cycle time and device yield and consequently to significantly gain in competitiveness in advanced technology manufacture for sub 65 nm technologies.

Project members:

2T102/E HYMNE		
ENDED	40-30	FR
	AIR LIQUIDE	FR
	ALCATEL ADIXEN	FR
	ALES	FR
	ATMEL ROUSSET	FR
	BEDE SCIENTIFIC INSTRUMENTS	UK
	CMP GC	FR
	ELDIM	FR
	FEI ELECTRON OPTICS	NL
	GEMETEC	DE
	ION - TOF	DE
	JOBIN YVON	FR
	KEMESYS	FR
	LETI	FR
	CNRS - LTM	FR
	M+W ZANDER	DE
	MASA	FR
	NETRAL	FR
	NXP SC	NL
	NXP SC	FR
	R2D	FR
	RECIF TECHNOLOGIES	FR
	SEZ	AT
	SI AUTOMATION	FR
	SOPRA	FR
	STMICROELECTRONICS	IT
	STMICROELECTRONICS	FR

Dates and Resources:

This project was scheduled to begin January 1st 2005 and actually began in February 1st 2005 and ended in January 31st 2009.

The original project lifetime of 36 months overran by 12 months.

Total manpower: 435 P.Y.

Status and Achievements:

The project progressed well overall after the change in the Crolles Alliance in 2007 and after NXP refocused its activities on Nijmegen. In the area of fabrication line management very innovative approaches were developed allowing cycle time and yield improvement. HYMNE was a multidisciplinary project and numerous publications have been issued over the project's lifetime.

2T103: FOREMOST

Objective:

The FOREMOST project developed advanced process modules and transistor architectures for a full CMOS 45 nm process and DRAM 50 nm technologies in European 300 mm manufacturing industrial facilities.

Project members:

2T103/B FOREMOST		
ENDED	AIR LIQUIDE	FR
	AIXTRON	DE
	ASM FRANCE	FR
	ASMI	NL
	FHG CNT	DE
	FREESCALE CROLLES	FR
	IMEC	BE
	IMEP	FR
	IMS NCSR	GR
	ION BEAM SERVICES	FR
	JORDAN VALLEY SC	IL
	LAHC	FR
	LETI	FR
	LMGP	FR
	LTM	FR
	MDM	IT
	NXP SC	BE
	NXP SC	FR
	QIMONDA	DE
	SAFC HITECH	UK
	STMICROELECTRONICS	IT
	STMICROELECTRONICS	FR
	VISTEC ELECTRON BEAM	DE

Dates and Resources:

This project began as planned in January 1st 2006 and ended in June 30th 2009. The original project lifetime of 30 months overran by 12 months .Total manpower: 657 P.Y

Status and Achievements:

Despite the big strategy changes of some of the main partners (Crolles 2 Alliance,) the LP CMOS045 platform and the DRAM technology steps have been completed on time, as scheduled more than 3 years ago. Thus, ST has been among the first manufacturers in the world to offer a 45 nm Low Power technology. The integration of improved solutions into the main core LP technology (like the GP transistors) and in the full DRAM process integration has been successfully achieved. The last big change in the economic environment that occurred at the beginning of 2009 had some impacts on the last steps of the project with Qimonda insolvency and priority change in ST customer requests.

The 45 nm process developed in FOREMOST project is the core process that is used worldwide for the wireless mobile applications. It enables a 50% reduction in chip area compared to the 65 nm node, and employs transistors that are substantially faster than anything ever previously fabricated. The exploitation of FOREMOST outcomes for materials producers and suppliers, equipment manufacturers are also promising. New products are now commercially available. The FOREMOST project was ranked second for the EUREKA innovation 2010 award.

2T104: DECISIF

Objective:

The objectives of this project are to integrate performance boosters in fully and partially depleted SOI technologies for Low Power and High Performance CMOS options to validate their impact by fabricating complex 45 nm node demonstrators directly comparable with bulk SI and to develop design kits and SOI-adapted circuit design for evaluation by application designers.

Project members:

2T104/E 2ML3 DECISIF		
ACTIVE	AIXTRON	DE
	DOLPHIN INTEGRATION	FR
	FZ JUELICH	DE
	GLOBALFOUNDRIES	DE
	LETI	FR
	MPI-HALLE	DE
	SILTRONIC	DE
	SOITEC	FR
	STMICROELECTRONICS	FR

Dates and Resources:

This project was scheduled to begin January 1st 2008 and actually began in July 1st 2008 and was schedule to end in December 31st 2010 and actually ended on July 31st 2011.

The original project lifetime of 36 months will overrun by 7 months.

Total manpower: 114 P.Y.

Status and Achievements:

French partners started at the beginning of the year 2008, while German partners started in August 2008.

The end date has been defined to be July 31st, 2011 for the whole consortium. The consortium has made an important decision to focus on UTBOX (ultra thin silicon on thin oxide) taking into account the decrease of interest in sSOI (strain SOI) and the impressive results obtained on other advanced substrates. This project is considered by the worldwide community of experts as one of the most innovative and promising More than Moore project.

2T201: NEMeSyS

Objective:

The goal of this project is to create technological advantage and add value to European technology and products by developing fully integrated technology platforms for the embedding NVM functions in sub-100nm CMOS based Systems-on-Silicon.

In the project a co-operation is proposed between Philips Semiconductors, STMicroelectronics, Infineon, Atmel, IMEC and Leti. Each company has a leading role in certain segments of the industry where non-volatile memory appears to be a common denominator.

Project Members:

2T201/D NEMeSyS		
ENDED	ATMEL ROUSSET	FR
	IMEC	BE
	INFINEON	DE
	LETI	FR
	NXP SC	BE
	NXP SC	DE
	NXP SC	NL
	NXP SC	FR
	STMICROELECTRONICS	FR
	STMICROELECTRONICS	IT

Dates and Resources:

This project began as planned in January 1st 2005 and ended in December 31st 2008. The original project lifetime on 42 months was met.

Total manpower: 311 P.Y

Status and Achievements:

This project has developed a fully integrated technology platform for the embedding of NVM functions in sub-100 nm CMOS. Good achievements were made and in particular the 90 nm embedded flash node qualification granted at ST by Q2 2008 was the industry's first 90 nm eFlash qualification worldwide. The added value to European technologies and products by developing fully integrated technology platforms for the embedding of NVM functions is largely used by European car makers as a competitive advantage. All partners achieved the qualification test on products. Innovative process modules and cell concepts were introduced preparing the next generations (65 nm and 45 nm nodes).The next generation of NVM embedded are the topics of the CATRENE project REFINED.

2T204: ELIAS

Objective:

The goal of the project is the development of tests and simulations based methodologies for accelerated prediction of lifetime under challenging conditions in automotive applications.

Project members:

2T204/D 2ML2 ELIAS		
ACTIVE	ATMEL NANTES	FR
	AUSTRIAMICROSYSTEMS	AT
	CADENCE DESIGN SYSTEMS	DE
	DAIMLER	DE
	EPSILON	FR
	INFINEON	DE
	LAAS	FR
	ON SEMICONDUCTOR	BE
	ROBERT BOSCH	DE
	STMICROELECTRONICS	IT
	TELEFUNKEN	DE

Dates and Resources:

This project was scheduled to begin January 1st 2007 and actually began in April 1st 2007 and was scheduled to end in September 30th 2010.

The original project lifetime of 36 months will overrun by 6 months.

Total manpower: 135 P.Y.

Status and Achievements:

Aging models have been implemented into the RelXpert simulation software developed by Cadence to fit the requests of the consortium. The ELIAS project supports the high emphasis of quality and reliability demands in the automotive market. Due to the economic crisis in 2009, many partners were not able to reach all the milestones for 2009 on time. A change request for 6 months project prolongation has been approved to complete the exploitation of the results. It is very important for the European semiconductor manufacturers to differentiate from these competitors and to keep the front edge. The ELIAS project secures the consortium leadership in the automotive semiconductor market providing optimized and verified methods and tools for highly integrated and highly reliable Smart Power products, allowing permanent monitoring of the production line and simulation of the reliability - already in the phase of circuit development.

The ELIAS project won the Jean-Pierre Noblanc Award for Excellence 2009 at the Nanoelectronics Forum 2009 in Noordwijk, Netherlands.

2T205: SPOT-2

Objective:

The project SPOT-2 is aiming at the development and comparison of new generations of Smart Power Technologies for use in emerging market segments for automotive and also for consumer applications.

Project members:

2T205/D 2ML2 SPOT-2		
ACTIVE	ATMEL ROUSSET	FR
	AUDI	DE
	BRUCO	NL
	CONTINENTAL	DE
	IMMS	DE
	INFINEON	AT
	INFINEON	DE
	LAAS	FR
	NXP SC	BE
	ON SEMICONDUCTOR	BE
	ROBERT BOSCH	DE
	SOITEC	FR
	TELEFUNKEN	DE
	TRIDENT MICROSYSTEMS (NXP SC)	NL
	UNI DORTMUND	DE
	UNI DRESDEN	DE
	UNI STUTTGART	DE
	UNI VIENNA - ISSE	AT
	X-FAB	DE

Dates and Resources:

This project was scheduled to begin in January 1st 2007 and actually began in April 1st 2007 and is on schedule to end in September 30th 2010.

The original project lifetime of 36 months will overrun by 6 months.

Total manpower: 258 P.Y.

Status and Achievements:

Several technology approaches will be explored and developed, which are based on a deep sub-micron BCD-MOS process, using bulk and innovative SOI substrate material, both positioned at the 180 nm and 130 nm lithography level. The new advanced Smart Power processing technologies will enable a new class of products, combining high performance computation and high power management capabilities. The different technological approaches will allow a direct comparison of performances and will lead the way to future research projects.

2T206: SIAM

Objective:

The project aims at the establishment of silicon technology platforms for emerging high frequency and mm-wave consumer applications like 77 GHz automotive radars, 60 GHz wireless networking (WLAN and WPAN) and 100 Gbit/s optical data communications.

Project members:

2T206/B 2ML3 SIAM		
ACTIVE	ACREO	SE
	CATENA MICROELECTRONICS	NL
	ERICSSON	SE
	FHG IMS	DE
	IEMN	FR
	LETI	FR
	PHILIPS RESEARCH	NL
	SP DEVICES	SE
	STMICROELECTRONICS	FR
	TU DELFT	NL

Dates and Resources:

This project began as planned in January 1st 2008 and ended in December 31st 2010. The original project lifetime on 36 months is on schedule to be met.

Total manpower: 137 P.Y

Status and Achievements:

Important progress has been made in each work-package. Studies are very promising. The millimeter-wave market is currently based on so-called III-V semiconductor technologies and so limited by high manufacturing costs, high power consumption and the limited integration scale of those technologies. This is changing rapidly, with silicon now being considered as the semiconductor material of choice to address such applications thanks to the high innovation level of the project results. Two types of silicon technology platform have been made available to compete with the above technologies and to allow the realization of System On a Chip that cannot be addressed with pure Bipolar technology:

- A millimeter-wave oriented 130 nm SiGe BiCMOS technology, featuring a 230/280 GHz fT/fmax SiGeC heterojunction bipolar transistor (HBT) and,
- A 65 nm low-power CMOS-SOI process, using 300 mm HR SOI substrates to allow for millimeter-wave designs with high quality passive devices.

A Change Request in June 2009 extends the SOI offer for RF and Mm-wave. This change will be focused on the development of additional devices that do not exist today on the 65nm ST SOI technology.

The number of publications submitted and accepted proves the innovative character of this project.

2T210: MaxCaps

Objective:

This project aims to develop new materials for memories and capacitors, which will be needed to fulfil future technology requirements. Concerning capacitors the main goal is to increase the capacitance per surface area, with very low leakage currents and excellent RF linearity to enable integration of currently discrete components into the chip. In the memory field DRAM structures and additionally new PCRAM materials to be deposited by means of (PE) ALD techniques will be evaluated.

The project encompasses the complete chain from basic materials (precursor) research, equipment development to incorporate the new materials and processes.

Project members:

2T210/B 2ML3 MaxCaps		
ACTIVE	AIR LIQUIDE	FR
	AIXTRON	DE
	ANALOG DEVICES	IE
	ASM FRANCE	FR
	ASM MICROCHEMISTRY	FI
	ASMI	NL
	BRONKHORST	NL
	IHP MICROELECTRONICS	DE
	IMEC	BE
	INFINEON	DE
	IPDIA	FR
	LETI	FR
	NXP SC	BE
	NXP SC	NL
	OXFORD INSTRUMENTS PLASMA	UK
	R3T	DE
	SAFC HITECH	UK
	STMICROELECTRONICS	FR
	ST TOURS / ST-F	FR
	TEMIC	DE
	TU EINDHOVEN	NL
	TYNDALL INSTITUTE	IE
	UNIVERSITY OF HELSINKI	FI

Dates and Resources:

This project was scheduled to begin in January 1st 2008 and actually began in February 12th 2008 and was scheduled to end in August 31st 2011.

The original project lifetime of 36 months will overrun by 8 months.

Total manpower: 124 P.Y.

Status and Achievements:

The project developed electrodes for future technology nodes memory applications. Some adjustment of milestones and deliverables are foreseen in 2010 due to the late approval and delay in Germany and the announcement of the NXP (Netherlands) to withdraw from the WP4 and WP5 activities at the end of 2009. A project extension of 9 months approved in the first half of 2010 will allow completing all tasks.

2T301: EAGLE

Objective:

The goal of the MEDEA+ project EAGLE is to develop in accordance with the targets the technology for a European EUV lithographic platform for volume manufacturing. This will enable the semiconductor industry to produce in 2009 in accordance to the ITRS roadmap, ICs for the 32 nm node. With respect to the alpha-demo tool developed in the preceding MEDEA+ project T405-EXTATIC, major new technological developments are required in the critical key sub-systems of the lithographic tool following the tool system architecture, viz. handling and sensor systems, optics and collector. Mentioned aspects will be integrated at the end of the project in order to demonstrate first light out of a system as well as the feasibility of the system and the technology target specifications.

Project members:

2T301/B EAGLE		
ENDED	ALCATEL VAC.TECH.	FR
	ASML	NL
	CARL ZEISS SMT	DE
	FOM - RIJNHUIZEN	NL
	MEDIA LARIO	IT
	PHILIPS EUV	DE
	SAGEM	FR
	XTREME TEC	DE

Dates and Resources:

This project began as planned in February 1st 2006 and was scheduled to end in December 31st 2008 and actually ended on June 30th 2009.

The original project lifetime of 32 months overran by 6 months.

Total manpower: 751 P.Y.

Status and Achievements:

EAGLE project ended on June 2009. The final milestone of the project (first light from the integrated system) has not been realised before the end of the project extension phase, because of delays of activities outside the project. This final milestone was shifted to Q2 2010. An updated Report will be provided after achievement of the final milestone. Nevertheless the outcomes of the EAGLE project are very promising:

The first tool, the NXE3100 was originally intended for 32 nm but progress in the past years with the Alpha Demo Tools, and in the field of optical components manufacturing has allowed ASML to offer it as a 27 nm tool to customers.

The EAGLE project has enhanced the possibility that Europe secures its world-wide leadership in the EUVL market. The EAGLE project paved the way for the EXEPT project from CATRENE 1st call started in February 2009 for the 22 nm node.

2T302: MUSCLE

Objective:

This project aims to develop means to control mask costs and to safeguard the European autonomy in masks for nano-electronics. It will combine broad common efforts from IC designers, mask makers, material providers, software houses and mask users in order to create a leading edge supply chain for very high advanced masks in a zero defect quality concept for final product.

Project members:

2T302/F MUSCLE		
ENDED	ALCATEL VAC.TECH.	FR
	ALTIS SC	FR
	AMTC	DE
	ASML	NL
	ATMEL ROUSSET	FR
	DCE	BE
	DMS	DE
	DNP PHOTOMASK	IT
	ENTEGRIS	FR
	ICADA	DE
	IMEC	BE
	INFINEON	DE
	LETI	FR
	NIKON	DE
	NXP SC	FR
	PHOTRONICS HELLAS	GR
	PHOTRONICS UK	UK
	QIMONDA	DE
	STMICROELECTRONICS	IT
	TOPPAN PHOTOMASKS	FR
	VISTEC	DE
	XYALIS	FR

Dates and Resources:

This project began as planned in January 1st 2005 and ended in December 31st 2007. The original project lifetime on 36 months was met.

Total manpower: 131 P.Y

Status and Achievements:

A comprehensive mask supply chain model has been developed that allows quantitative analysis of parameters impacted by changes and improvements in the supply chain. All parameter steps were set up and agreed upon by the consortium. Mask order flow has been unified and proposals prepared for international standardization.

2T304: LIQUID

Objective:

The LIQUID project addresses the development of Immersion lithography and will enable the semiconductor industry to produce 50 nm features with optical lithography, possibly extendable towards the sub 45 nm region.

Project members:

2T304/E LIQUID		
ENDED	ASML	NL
	CARL ZEISS SMT	DE
	COHERENT	DE
	FREESCALE CROLLES	FR
	IMEC	BE
	INFINEON	DE
	LETI	FR
	LTM	FR
	NXP SC	FR
	NXP SC	BE
	PHOTRONICS FRANCE	FR
	PHOTRONICS UK	UK
	QIMONDA	DE
	SCHOTT LITHOTEC	DE
	STMICROELECTRONICS	FR
	TUILASER	DE

Dates and Resources:

This project began as planned in January 1st 2005 and ended in December 31st 2008. The original project lifetime on 42 months was met.

Total manpower: 504 P.Y

Status and Achievements:

The project covers all basic aspects of the involved technology: the lithographic exposure tool with laser and optics, the reticles and the processes and required metrology. The project includes also the development of most critical materials like Fused Silica, CaF2 and immersion liquids.

The first 45 nm tools have been shipped and customers use it in mass production environments. The first extension system towards the 38 nm node (single exposure) passed the qualification test positively. Zeiss and ASML abandoned the start of a product development of high index immersion lens and system because there is no longer a market for such a system. This project has enhanced the possibility for European lithography related industry to maintain and improve their worldwide competitive position. This project has strongly contributed to the deployment of the immersion technology world wide for the most advanced More Moore CMOS technologies.

2T305: FANTASTIC

Objective:

The FANTASTIC project addressed the development and assessment of UV-Nanoimprint lithography for high resolution and high throughput microelectronic applications. Nanoimprint technology has claimed to be a competitive candidate for Next Generation Lithography due to its advantages concerning resolution and cost effectiveness.

Project members:

2T305/A FANTASTIC		
ENDED	AMO	DE
	AMTC	DE
	ASML	NL
	DNP PHOTOMASK	IT
	EVG	AT
	FHG CNT	DE
	FHG ISC	DE
	IMEC	BE
	IMS CHIPS	DE
	INFINEON	DE
	LETI	FR
	LTM	FR
	MICRO RESIST TECHNOLOGY	DE
	MOLECULAR IMPRINTS	FR
	NAWOTEC	DE
	NXP SC	BE
	QIMONDA	DE
	STMICROELECTRONICS	FR
	VISTEC	DE

Dates and Resources:

This project began as planned in July 1st 2006 and was scheduled to end in June 30th 2008 and actually ended on September 30th 2009.

The original project lifetime of 24 months overran by 15 months.

Total manpower: 101 P.Y.

Status and Achievements:

The template inspection and repair tool have a promising future for the most advanced CMOS technologies. It turned out that modifications and continuous improvement of the existing step and repeat system EVG770 will not lead to the targeted 32 nm node and beyond specifications. A completely new tool with promising capabilities was designed and built within the scope of the FANTASTIC project (EVG770 Generation II). Important progresses have been done (template fabrication and repair, printable low-k…) but blocking points have not been removed (CD control and dispersion, throughput too low, CoO not acceptable, defectivity issues not solved). The imprint technology will be used for other applications than advanced CMOS technology nodes (Light Extraction in LED, Lens arrays in wafer level cameras, photo voltaic, LCD, architecture holograms, polymer electronics…

2T307: CRYSTAL

Objective:

Project goals are to decrease cycle time excursions and to simplify mask qualification procedures for the 193 nm lithography supply chain.

Innovative deliverables from work packages are a photomask DFM methodology Standard, an integrated contamination control plan and an innovative photomask qualification procedure.

Expectations are to improve related present current metrics by 50%.

Project members:

2T307/A 2ML3 CRYSTAL		
ACTIVE	ALCATEL VAC. TECH.	FR
	AMTC	DE
	ASML	NL
	ATMEL ROUSSET	FR
	CARL ZEISS SMT	DE
	DMS	DE
	ECP	FR
	LETI	FR
	LTM	FR
	SATIN IP	FR
	STMICROELECTRONICS	FR
	TOPPAN PHOTOMASKS	FR
	XYALIS	FR

Dates and Resources:

This project began as planned in January 1st 2008 and will end in December 31st 2010. The original project lifetime on 36 months is on schedule to be met.

Total manpower: 86 P.Y

Status and Achievements:

The project progressed as planned. The benchmark of DFM masks has been initiated and the demonstrator prototype has been presented and improved. The study of contamination and defects and the modeling to evaluate the process window of mask qualification have started with exchange of statistical data between all the partners. The consortium promotes the qualifications methods and process flow as standards. The CRYSTAL partners have achieved Milestones in average at project level which fits with the project position in the timeline. The commercial exploitation already started mainly from WP2 results/activities (WP2: Mask Material Flow).

2T401: HI-MISSION

Objective:

The overall objective of HI-MISSION is to develop innovative technology and design platform for RF Microsystems applications. The platform will enable a flexible microwave design, decreasing substantially the new product development time and facilitating new concept verification. The tunable devices will also enable the reuse of existing devices in new applications

Project members:

2T401/F HI-MISSION		
ENDED	ACREO	SE
	ERICSSON	SE
	INFINEON	AT
	INFINEON	SE
	SAAB MW	SE
	SP DEVICES	SE
	STMICROELECTRONICS	FR
	UMS	FR

Dates and Resources:

This project was scheduled to begin January 1st 2005 and actually began in October 24th 2005 and actually ended on April 30th 2009.

The original project lifetime of 36 months overran by 6 months.

Total manpower: 81 P.Y.

Status and Achievements:

The main goal to develop a technology platform for RF SiP/SoC Applications in the field of automotive, military radar and microwave communication systems has been achieved. HI-MISSION proposed new solutions for very integrated, low cost and flexible millimetre-wave front-ends.

The interconnections developed with HI-MISSION have been adapted to customers for automotive market, and a very good feed-back has been also received for telecommunications, defence and space markets.

The first developments of ASICs around the technologies developed with HI-MISSION project have started in 2009 for some major customers. These solutions have been proposed as UMS standard in 2010.

2T405: CoSiP

Objective:

The objective of this project is to provide the enabling basic design environment required for the creation of a wide variety of compact systems. It is also to create an adequate design environment for SIP, involving the complete chip/package/board system which does not exist.

Project members:

2T405/A 2ML3 CoSIP		
ACTIVE	CISC SEMICONDUCTOR	AT
	DOCEA	FR
	INFINEON	AT
	INFINEON	DE
	IRSEEM	FR
	MAGWELL	BE
	ROBERT BOSCH	DE
	STMICROELECTRONICS	FR

Dates and Resources:

This project was scheduled to begin January 1st 2008 and actually began in June 6th 2008 and will actually end on December 31st 2011.

The original project lifetime of 36 months and will overrun by 6 months.

Total manpower: 87 P.Y.

Status and Achievements:

The consortium aims at shorter time to market, shorter redesign cycles, and more reliable design and products.

The project started officially in June 2008. This first and half year was covered with significant obstacles caused by the different starting dates of the project in the different countries. A common end date was set to December 2011.

The CoSip project is the first project world-wide where several partners work together to develop a coherent and collaborative chip-package-board co-design method.

2. MEDEA+ PROJECTS IN APPLICATIONS

2A103: MIMOWA

Objective:

The project focussed on LTE and WiMAX and main research advances have been initiated.

The MIMOWA project has significantly closed the gap between academic research of multiple antenna systems and the implementation of algorithms and system components for base stations and terminals.

The project dealt with the specification of MIMO building blocks, algorithms and modelling, detailed and in-depth knowledge of how software and hardware could be implemented, MIMO IP blocks, MIMO system architecture of transceivers, antennas; RF-frontends; converters; and digital baseband.

Project Members:

2A103/A MIWOWA		
ENDED	AGILENT	BE
	ALCATEL - LUCENT	DE
	AWE COMMUNICATONS	DE
	CTTC	ES
	CUAS	DE
	INFINEON	DE
	NSILITION	BE
	OMP	BE
	RUNCOM	IL
	STMICROELECTRONICS	BE
	STMICROELECTRONICS	TR
	TELEFONICA I&D	ES
	UCL	BE

Milestones and Resources:

This project was scheduled to begin in 01 January 2007 and actually began in 22 February 2007. The original project lifetime of 27 months was extended by 1 month and 121 PYs were employed.

Status and Achievements:

Until project end, more than 40 publications in conferences and journals were achieved. The IP being created led to 9 new patents being filed or granted during the project lifetime. Contributions to standardisation could be given by some of the partners to IEEE 802.16 and 3GPP/LTE RAN1 and RAN2.

Furthermore, most of the industrial partners could transfer major parts of the project results into the development process of ongoing and future products.

2A105: SR2 (Short Range Radio)

Objective:

When the Witness project (MEDEA code A109) finished, the main conclusion was that it is not possible to choose one wireless technology, over the other ones, in order to implement a global application Network. Every technology has its pros and cons, and different scenarios could mean different solutions.

One of the objectives in the SR2 project is to develop multi-mode and multi-standard solutions, which make it possible to have Networks where different technologies interact and coexist.

In addition, developed devices are to be used in BAN context, so they have to achieve, apart from low power consumption, low power radiation and antennas which operate correctly when placed on the human body.

Project Members:

2A105/C 2ML3 SR2		
ACTIVE	ADD	ES
	AICIA	ES
	CEIT	ES
	CISC SEMICONDUCTOR	AT
	FAGOR	ES
	IKERLAN	ES
	IMSE - CNM	ES
	IUMA	ES
	NXP SC	BE
	ST-ERICSSON	BE

Milestones and Resources:

This project was scheduled on 01 January 2008 until 31 December 2010. This project started on time but had a lot of start up problems because of funding problems in several countries. This resulted in a reduction of partners from 17 to 10, person years from 219 PYs to 111 PYs and of project specifications and into an extension of the project by one year.

Status and Achievements:

Application requirements and scenario definition, and the report on state-of-the-art on technologies and techniques have been finished. Bluetooth System specification and the report on architecture concepts and selection were finalized. Building block and system specification is ready.

The development of an adaptation layer for BT profiles to Wimedia UWB radio has been completed with some advance in the planning.

With respect to the work on the 802.15 technologies in WP3, System Specification, report on architecture concepts and selection, and Building block and system specification have been finished during the year as scheduled. Also a significant amount of work has been devoted to chip design in order to meet the deadline of the deliverables to be produced in 2010.

The project is expected to end 31 December 2011.

2A106: Qstream (Ultra-high Data-rate Wireless Communication)

Objective:

The Qstream project aims at successful realization of low-cost, highly-integrated, ultra-high-data-rate streaming applications operating in the mm-wave frequency range. Complete receiver and transmitter ICs (RF and digital baseband) will be realized in CMOS technology, in addition to System-in-Package (SiP) implementations enabling mm-wave front-ends containing antenna arrays and active chips on a low-cost substrate. The validity of the chosen concepts will be demonstrated by two functional prototypes.

Project Members:

2A106/C 2ML3 Qstream		
ACTIVE	CYNER SUBSTRATES	NL
	IAF	DE
	IEMN	FR
	IMEC	BE
	IMS LAB	FR
	LAAS	FR
	LEST	FR
	LETI	FR
	NXP SC	BE
	NXP SC CROLLES	FR
	SIGNAL GENERIX	CY
	STMICROELECTRONICS	IT
	STMICROELECTRONICS	FR
	THECHNICOLOR	FR
	TRIDENT MICROSYSTEMS (NXP SC)	NL
	TU BRAUNSCHWEIG	DE
	TU EINDHOVEN	NL
	TU KAISERSLAUTERN	DE

Milestones and Resources:

This project was scheduled to begin on 01 January 2008 and actually began on 01 April 2008. The original project lifetime of 36 months most probably will be met with the 171 PYs planned.

Status and Achievements:

The project is on track. The project has a strong dissemination: A lot of papers were published and significant participation in conferences has been reported. The project showed strong participation in standardisation. Three patent IDs were submitted.

The benefits of the results and outcomes of this project will consist on exploiting the experience and know-how acquired during the project on 60 GHz design, to develop a chip set for the HDMI cable replacement by a wireless link at 60 GHz. A second target is to reduce the total power consumption of the RF part by a factor 5, compared with current power figures from the competition, thanks to the Qstream RF unique architecture for System 2.

2A201: BLAZE

Objective:

This project aims at boosting the European semiconductor, consumer electronics and content distribution industry in order to become leading in the high definition media distribution and storage market through advanced co development.

This will be based on an innovative storage standard called BLU RAY that is currently under development.

Project Members:

2A201/C BLAZE		
ENDED	DATARIUS	AT
	LAG	FR
	LETI / MPO	FR
	NXP SC	NL
	NXP SC	FR
	PHILIPS APPLIED TECHNOLOGIES	NL
	PACE FRANCE	FR
	STMICROELECTRONICS	FR
	THOMSON R&D	FR

Milestones and Resources:

This project was running from 01 January 2005 until 31 March 2008 and used 426.5 PYs.

Status and Achievements:

Compared to the Asian Competitors the BLAZE project is able to show substantial results: a single SoC solution (ST7200) which makes the HW more cost effective. The ST7200 is the first cost-optimized solution.

Use of latest silicon technology 65 nm process (smaller chip and lower power consumption).

The investment in the Multi Standard Video Decoder is enabling an even more economic SoC solution in the future. With the same IP 5 different technology areas can be targeted.

The realized Stamper tester is the industries first solution that increases yield and decreases costs of disc production (competitive to HDDVD).

This project has a lot of innovations (important patents have been filed) with exploitation of all industrial partners and institutes. A spin-off at LETI for mask less lithography is in preparation, indicating that the technologies developed in BLAZE leveraged these new opportunities.

The Blaze project won the Jean-Pierre Noblanc Award in 2008.

2A202: UPPERMOST

Objective:

UPPERMOST will research, develop and demonstrate cost-effective, low-power, highly adaptive and reconfigurable technical solutions for future mobile terminals, by conducting studies at system, sub-system (i.e. radio architecture) and component levels.

The main focus of the UPPERMOST project is the study of

- Reconfigurable radio front-end (multi-mode & mult-band)
- Reconfigurable power efficient baseband architecture
- Lower Level protocol (mainly PHY and DLC layers)
- Generic Power supply strategy for reconfigurable architecture

Project Members:

2A202/B UPPERMOST		
ENDED	AGILENT	BE
	IMEC	BE
	IMS LAB	FR
	KUL - ESAT	BE
	LETI	FR
	MOTOROLA	FR
	NXP SC	FR
	NXP SC	BE
	STMICROELECTRONICS	BE
	STMICROELECTRONICS	FR
	TCT	BE

Milestones and Resources:

This project started 01 January 2005 and ended 31 December 2007 according to schedule and within the planned 199 PYs.

Status and Achievements:

The project achieved a high degree of innovation.

Software-defined radio system technology ready to meet global challenges: Development of software-defined radio systems and software-like architectures in the UPPERMOST project offers flexibility and efficiency in the development of highly integrated, reconfigurable multimode mobile systems and equipment. The results of this highly innovative project are already influencing the evolution of multimode and multistandard mobile terminals towards heterogeneous wireless network environments from cell phones to mobile television, supporting new standards and keeping Europe in the vanguard of global advances in wireless communications against tough US and Asian competition.

2A204: SWANS

Objective:

The goal of the project SWANS is to define a common toolbox, aiming at integrating analogue and digital IP blocks for future wireless sensor nodes. This common toolbox will be used to demonstrate functional IP blocks, macro cells and chipsets for 5 application classes: aeronautic, health/fitness, homeland security, automotive and environmental monitoring.

Project Members:

2A204/C SWANS		
ENDED	AIRBUS	FR
	ANSEM	BE
	ATMEL ROUSSET	FR
	CORONIS SYSTEMS	FR
	EADS CRC	FR
	EADS SN	FR
	ENERGO CONTROL	PL
	SIGTEL	FR
	FRANCE TELECOM R&D	FR
	IMEC	BE
	IMS	FR
	LETI	FR
	LMS	BE
	LMS INSTRUMENTS	NL
	NXP SC	BE
	PRO ENGIN	FR
	STMICROELECTRONICS	FR
	VERHAERT	BE

Milestones and Resources:

This project was scheduled to begin on 01 January 2005 and actually began on 14 March 2005.

The original project lifetime of 36 months needed an extension of 5 months. The project had a work content of 162 PYs.

Status and Achievements:

Combining wireless networking and sensing in one package: Wireless access to the Internet and wireless headsets for mobile phones are now established facilities. However, there are many other applications in which autonomous wireless networking has growing potential – from remote utility metering to stress monitoring in aircraft. The ability of wireless sensor devices to maintain connections to their networks and to perform sensing activities autonomously is an ever-increasing requirement that the SWANS project has successfully resolved with the development of technology that allows the wireless and sensing circuitry to be combined in a single package.

2A206: ASIC-CCD

Objective:

This project aims at strengthening the European capabilities for systems-on-silicon for future imaging applications. The project intends to reach this by establishing strategic know-how for the European industry in the field of high-end CCD imagers and video processing for applications in professional broadcast, machine vision, medical, digital photography and other markets. The project focuses on the (pre-competitive) research and advanced development phase, thus resulting in intellectual property on how to increase the frame rate in CCD imagers maintaining the high resolution, in a flexible video processing architecture, in prototype IC's, and prototype systems, including interconnect and networking architectures. These will form a good base for development of advanced products.

Project Members:

2A206/B ASIC-CCD		
ENDED	ADIMEC	NL
	DALSA	NL
	EQCOLOGIC	BE
	GRASS VALLEY FRANCE	FR
	GRASS VALLEY NEDERLAND	NL
	TU DELFT	NL

Milestones and Resources:

This project started on 01 January 2006 and ended 30 June 2008 according to schedule using 57 PYs.

Status and Achievements:

The project partners had influence in a number of standardisation bodies. A lot of project results are already incorporated in new products.

Slow-motion in high definition: A limitation with the introduction of high-definition (HD) broadcast TV and other HD imaging systems has been poor quality slow-motion replay. The reasons for this were attributed to the constraints of the charge-coupled device (CCDs) imagers and supporting circuitry in the cameras. The ASIC-CCD project developed new image-capture sub-systems to address these issues. The first products were demonstrated during the UEFA soccer championship in June 2008. This continuing development work has now put European manufacturers of HD image-capture sub-systems in a leading position on the world stage.

2A207: TritonZ

Objective:

TritonZ brings together technology suppliers for the imaging chain in the broadcast (consumer entertainment) and industrial markets. The project concentrates on the image capture part of the chain including transmission and on-set pre-visualization.

Developments towards higher spatial resolutions will take place for 2D image capture, but these will also prepare the creation of multi-view image capture. Anyway, the bandwidth needed throughout the chain will (have to) increase, and this trend will be used to first extend beyond HDTV in 2D and second to move to 3D by adding depth and occlusion information to the regular 2D output.

On the consumer side, thanks to powerful compression algorithms and the fact that only the authored version is distributed, Blu-ray is expected to be the right format for high volume diffusion. The standardization of the interface is still on-going, will use HDMI and may be stereoscopic for the first generation and 2D + depth for later generations.

The trends described above for broadcast also take place in machine vision. Both spatial and temporal resolution still have to increase for applications where vision is used to measure small details in production processes, position components with high precision and high speed in assembly processes and so on. Also in machine vision 2D+Z will have added value, as it will enable the control of positioning components in assembly processes in 3-dimensional space.

Project Members:

2A207/E 2ML3 TritonZ		
ACTIVE	ADIMEC	NL
	CMOSIS	BE
	EQCOLOGIC	BE
	GRASS VALLEY NEDERLAND	NL
	TRIDENT MICROSYSTEMS (NXP SC)	NL

Milestones and Resources:

This project started on 01-01-2009 and its planed end is 31-12-2010 using 41 PYs.

Status and Achievements:

The project progress is on schedule and all remaining partners are cooperating in a very constructive and open manner with each other. Hardware, from the first two modules for high data rate image capture, is ready and functional. The first demonstrators, using the CoaXPress digital interface, have been shown. Exploitation and dissemination is progressing very well. CoaXPress won the Vision Award, 2009.

Exploitation: Grass Valley: New camera head in 2H2011; Trident will sell rendering IP; Adimec: 20 Gbps camera platform in beginning 2011; First CoaXPress product to be shown on Vision Show Nov 2010 in Stuttgart; CMOSIS will demonstrate 12M pixel at Vision Show in Nov 2010; EqcoLogic will provide samples of frame grabbers in 2010.

2A208: iGLANCE

Objective:

The iGLANCE project brings a strong partner in advanced imaging with the European market leader of TV chips together in their ambition to realize new innovations in digital TV platforms.

This embedded system will be implemented by developing an innovative chipset and the corresponding software and architecture, where;

1. The system can offer the ultimate HDTV AV quality to serve the European mass-market application of HDTV, and by
2. Establishing a flexible architecture extension providing the additionally required computation power for 3D multi-view decoding, requiring the processing of several HDTV channels.

Project Members:

2A208/C 2ML3 iGLANCE		
ACTIVE	4D VIEW SOLUTIONS	FR
	INRIA	FR
	LOGICA	FR
	PHILIPS HEALTHCARE	NL
	PRODRIVE	NL
	SILICON HIVE	NL
	STMICROELECTRONICS	FR
	TASK24	NL
	TIMA	FR
	TU EINDHOVEN	NL
	VERUM	NL

Milestones and Resources:

This project was originally scheduled from 01 January 2008 until 31 December 2010. Because of a late start (01 October 2008) due to late funding decision the whole project has been moved by 9 months. The work content is 138 PYs.

Status and Achievements:

During 2009, progress has been made mainly in WP1 (Specifications of the System), WP2 (Study and Development of the iGlance System on Chip), and WP4 (Middleware). WP3 (FPGA for 3D rendering and Interfaces), as well as, WP5 (Demonstrator) have been partially addressed.

Due to the 3D market evolution during this period, the withdrawing of PHILIPS 3D Solutions from the 3D auto-stereoscopic panels and late availability of the PCA, some adaptations and changes have been made. The middleware layer of the iGlance platform has also been adapted to the new situation. Finally, during this year, a first version of the iGlance SoC was specified, developed and manufactured in a 65 nm technology node.

In terms of standardization, the iGlance first studies have also revealed the advantages of this L+R format compared to the 2D+depth.

Significant dissemination has been realised.

2A302: ONOM@TOPIC+

Objective:

The project's primary goal is to develop complete HW and embedded SW platforms, that will enable the European Community (Industrial or Government Operators, Terminals and Smart-cards companies, Silicon vendors) to take full profit of the enormous potentialities offered by the development of fixed or mobile e-Services.

Project Members:

2A302/B ONOM@TOPIC+		
ENDED	AXALTO	FR
	COMPUWORX	HU
	ESTEREL TECHNOLOGIES	FR
	GEMPLUS	FR
	ID3 SEMICONDUCTORS	FR
	LETI	FR
	NXP SC	FR
	OBERTHUR CARD SYSTEMS	FR
	OKSYSTEM	CZ
	ORANGE	FR
	PHILIPS-IC LAB	NL
	PRECISE BIOMETRICS	SE
	PURPLE LABS	FR
	SAFELAYER SECURE COMMUNICATIONS	ES
	STMICROELECTRONICS	FR
	TELEFONICA I&D	ES

Milestones and Resources:

This project started 01 April 2005 and ended 31 December 2007 according to schedule and used 281 PYs.

Status and Achievements:

The project has brought three major contributions to world standards that will enable to completely reshape the respective application targets addressed by the project;

On the Citizenship aspects, decisive contribution has been made that will enable the development of pan-European interoperable e-identity smart-card platforms compatible with most e-identity projects under preparation in most European countries such as France, Germany, Spain or United Kingdom.

On the Mobile Multimedia side the USB proposal has become an international ETSI/3GPP standard. The SWP proposal was the only one that enabled a SIM card to handle simultaneously both a High Speed Protocol and an NFC contact-less protocol. Onom@Topic+ has already received recognition through the receipt of MEDEA+ 'Jean-Pierre Noblanc' award in 2007, the Isabelle Attali award in 2007, the Global Frost & Sullivan Award for Emerging Company of Year 2008 and the Eureka innovation award 2010.

2A303: BioP@ss (Biometric Platform for next generation contact-less IAS)

Objective:

The BioP@ass project targets the development of advanced (microelectronics and embedded SW) secure and interoperable smart-card platforms for all needed e-administrative applications requested at European level. It assembles a powerful consortium including semiconductor manufacturers, card vendors, SW developers and integrators, mixing large industry, SME and academic partners. It will deliver several innovative options such high-speed contact-less interfaces, advanced biometrics, NFC connectivity that will enable the delivery to citizens of innovative services from a personal e-ID platform. It will leverage on the results of the former Onom@Topic+ MEDEA+ project and especially reuse the open middleware architecture proposed by the Consortium partners and currently under approval by some standardization committees.

Project Members:

2A303/C 2ML3 BioP@ss		
ACTIVE	COMPUWORX	HU
	G&D	DE
	GEMALTO	FR
	ID3 SEMICONDUCTORS	FR
	INFINEON	DE
	LETI	FR
	NXP SC	DE
	NXP SC CROLLES	FR
	OKSYSTEM	CZ
	PRECISE BIOMETRICS	SE
	STMICROELECTRONICS	FR

Milestones and Resources:

This project was scheduled starting 02 January 2008 ending 31 December 2009. The real start was 02 July 2008 due to late funding decision and the end date is now planned to be 30 January 20011. The planned resources for the project are 129 PYs.

Status and Achievements:

First versions of use cases were produced and shown during the September project review.

All industrial partners will introduce project results in their future offer • Gemalto, smart-card platform implementing IAS ECC applet and SAC for MRTD and Web server solution offers • G&D: smart-card platform and solution offers • Infineon Technologies, STMicroelectronics, NXP semiconductors: dedicated chips for serving the security market • CompuWorx, OK System: enhancement of SW offer, support to national programme • ID3 semiconductors, Precise Biometrics: development of their open Biometry component offer • Id3 Semiconductors is building a new product able to leverage developments in biometry and contactless. Prototypes are expected by Q4 2010.

2A401: Car-Vision

Objective:

The objective of this project was the creation of new type of image sensors, sensor packages, image processor and software to address the main EU concern of automotive safety. The driving assistance is one of the key topics.

Project Members:

2A401/C CAR VISION		
ENDED	CTAG	ES
	FICOSA	ES
	LETI	FR
	LIST	FR
	STMICROELECTRONICS	FR
	ULIS	FR

Milestones and Resources:

This project was originally scheduled from 01 January 2005 until 31 December 2007. It really started 01 April 2005 and ended 30 June 2008. The late start of the project was due to funding decisions and the extension by 2 months was due to late deliveries within the project. The project used 121 PYs.

Status and Achievements:

The exploitation of this project will have significant impact in supporting the European electronics automotive industry for designing cameras in vehicles.

Main highlights are the generation of three working imaging chips, two sensor packages, one imaging processor emulation platform and three working applications (software). Two of the applications, Lane Departure Warning and Blind Spot Detection were validated in real conditions inside various cars.

There is strong market relevance in the project mainly in the area of sensor domain. The business perspectives are good and several industrial partners have clear business plans.

Optical sensor system development set to improve safety on Europe's roads: The rapid growth in advanced driver-assistance systems has generated a number of in-car devices aimed at cutting traffic accidents, either by providing information or through direct intervention in vehicle control. The MEDEA+ 2A401 Car Vision project has now developed the basic components required for integration of in-car visual data that can assist with the avoidance of collisions in any type of conditions. The result is a cost-effective CMOS-based vision system platform and associated software that can be integrated in low-/medium-level vehicles to improve the safety of all road users.

2A403: Caring Cars

Objective:

It is the main goal of the Caring Cars project to increase car safety by enabling wellness applications in an automotive environment.

Project Members:

2A403/B Caring Cars		
ENDED	ATMEL NANTES	FR
	DEIMOS SPACE	ES
	EADS DS	FR
	ELBAU	DE
	GRUNDIG	TR
	IMTEK	DE
	MICRONAS SEMICONDUCTOR	DE
	MOBILERA	TR
	NXP ICLAB	NL
	PHILIPS APPLIED TECHNOLOGIES	NL
	PHILIPS RESEARCH	DE
	ROBOTIKER	ES
	SIEMENS AG	DE
	SIEMENS VDO AUTOMOTIVE	DE
	TELEFONICA I&D	ES
	TOFAS	TR
	UC3M	ES
	UNI TUEBINGEN	DE

Milestones and Resources:

This project was originally scheduled to begin on 01 October 2006 and to end on 30 September 2009. Due to negative funding decisions the starting date moved to 01 June 2007 and the end date to 31 December 2009. The project had to be reduced in number of partners (19 → 9), in deliverables (65 → 40) and capacity (262 → 125 PYs). The project was totally reorganised without changing the objective.

Status and Achievements:

The project realised an open automotive infrastructure, the basis of which has been formed by a sensor network in cooperation with a car gateway. This sensor network consist of the sensors already available in vehicles augmented with new sensors. The Car gateway establishes a connection with the external world signalling for instance emergency services. In this way it is possible to improve car safety and thus reduce the costs of transportation. By adding external communication to the infrastructure envisioned by the project it will also become possible to use the same infrastructure to support health care applications.

2A502: TSC

Objective:

The Trusted and Secured Computing (TSC) project aims at developing a family of HW/embedded SW silicon components enforcing secure and trusted computing in the Consumer, Computer, Telecommunications and Wireless areas.

It also intends to develop trust concept and architecture elements usable in other European industrial segments such as automotive, industrial, aeronautics (especially in their content acquisition and payment, ticketing and DRM aspects).

Project Members:

2A502/A TSC		
ENDED	AXALTO	FR
	BERTIN TECHNOLOGIES	FR
	BULL	FR
	CELESTICA VALENCIA	ES
	CMP GEORGES CHARPAK	FR
	EADS DS	FR
	EADS SN	FR
	ESI	ES
	FRANCE TELECOM R&D	FR
	LETI	FR
	LIP6	FR
	PHILIPS APPLIED TECHNOLOGIES	NL
	STMICROELECTRONICS	FR
	TB SECURITY	ES
	TB SOLUTIONS	ES
	TECHNIKON	AT

Milestones and Resources:

The original schedule of this project was from 01 January 2006 until 31 December 2008. Due to funding problems the project schedule and the consortium had to be changed. It started 01 September 2006 and ended 30 December 2009 with a consummation of 203 PYs.

Status and Achievements:

The TSC project was launched as a European initiative to counter the US dominance in the Trusted Secure Computing area. It aimed at bringing Europe its strategic independence in this sovereignty or high-potential area.

The TSC Consortium reached this objective and at the end of the project the HW and SW components were available. These components were integrated in several demonstrators showing unprecedented capabilities in the global security area. These concepts and products are already helping Europe develop its own trusted-computing facilities interoperable with international standards.

2A701: Parachute

Objective:

Considerable steps forward have to be made to improve the Reliability of Applications based on these Electronic Systems. Reliability will be defined here as the securing of the system function regardless the presence of Interference and these Parasitic Effects. The one that will especially be considered are: Electromagnetic Reliability due to the presence of electromagnetic parasitic effects: Electromagnetic Compatibility (EMC), Power Integrity, Signal Integrity, Short Electrical Transient, electrostatic discharges, and Particle Radiation Reliability.

Project Members:

2A701/B PARACHUTE		
ENDED	AIRBUS	FR
	AMIS	BE
	ATMEL NANTES	FR
	ASTRIUM ST	FR
	ASTRIUM ST	DE
	BIU	ES
	EADS CRC	FR
	FREESCALE	DE
	INFINEON	DE
	IROC TECHNOLOGIES	FR
	PHILIPS APPLIED TECHNOLOGIES	NL
	ROBERT BOSCH	AT
	ROBERT BOSCH	DE
	STMICROELECTRONICS	FR
	THALES ALENIA SPACE	ES
	TEMIC	DE
	TIMA	FR
	UC3M	ES
	UNI PADERBORN	DE
	ZUKEN	DE

Milestones and Resources:

This project was scheduled to begin 01 January 2005. It started 01 April 2005 due to funding decisions. The planned end date was 31 December 2007. Due to very late starting companies in one member country due to funding decision in this country the project had to be extended to 31 March 2009. The capacity in the project was 307 PYs.

Status and Achievements:

New EMR modelling techniques improve design of entire microelectronics subsystems: The methodologies developed within the MEDEA+ PARACHUTE project are applicable to testing for both electromagnetic interference and particle radiation, and will help ensure Europe retains its ability to stay at the leading edge of advanced microelectronics for the automotive and avionics industries.

2A702: NanoTEST

Objective:

The NanoTEST project targets breakthroughs in manufacturing test, in the area of costs as well as in achieved quality and time-to-market.

At the start of the project the NanoTEST project consortium defined some very aggressive goals for creating breakthroughs in manufacturing test: Low cost: 10X; Improved quality: 0ppm; Shorten Tim-to-Market: 10X.

These goals should be achieved by introducing advanced test methodologies for SoC and SiP test. Furthermore, the project would focus its activities on development of test flows, tools and standards.

Project members:

2A702/D NanoTEST		
ENDED	AMIS	BE
	INFINEON	AT
	INFINEON	FR
	LETI	FR
	LIRMM	FR
	NXP SC	FR
	NXP SC	NL
	PHILIPS	NL
	QSTAR TEST	BE
	STMICROELECTRONICS	FR
	TEMENTO SYSTEMS	FR
	TIMA	FR

Milestones and Resources:

This project started 01 January 2005 and ended 31 December 2008 according to schedule. Resources employed were 392.5 PYs.

Status and Achievements:

All project milestones targeted have been achieved.
Cost / test time: Up to 20x in digital test; More than 10x in memory testing; Up to 4x in AMS test (parallel concurrent testing enabled by DfT and BIST); Up to 4x in RF testing - this can not be shown statistically by too little data points.

Quality: Zero-defect programs are in place and effective in all IDMs.
TTM improvement: 50% reduction.

The overall innovation level of the NanoTEST project is best shown by over 300 papers in total that have been submitted and presented at key scientific conferences, such as DATE, ITC, VTS, ETS.
The project received the IET Ambition and Achievement Awards 2008.

A number of best paper awards were received during project duration. The NanoTEST consortium submitted some 25 IDs re. new test methodologies for SoC and SiP test. NanoTEST partners were heavily involved in standardization activities, like IEEE1149.4, P1149.7, AEC-Q100, STIL_AMS ...

2A703: NEVA

Objective:

With circuit size potentially reaching one billion transistors by end 2008, traditional bus-based single-clock architectures become unusable for commercial circuits. Starting from successful design approaches (e.g. Multi-Processors, Asynchronous Design) proven during MEDEA+ phase-1, NEVA intends to raise 3 main innovations up to industrial level: communication-centric design for fast simulation and execution, infrastructures for real-time applications, and a complete design flow to implement asynchronous techniques. Datastream applications, mainly from the Video field, will be used as drivers, with a target computing power of 1 GOPS per chip.

Project members:

2A703/C NEVA		
ENDED	ACE	NL
	BULL	FR
	FRANCE TELECOM	FR
	LETI	FR
	NXP SC	NL
	STMICROELECTRONICS	FR
	TIMA	FR
	UNI LEIDEN - LIACS	NL
	VERIMAG	FR

Milestones and Resources:

This project was scheduled and executed from 01 January 2005 until 31 December 2008 using 280 PYs.

Status and Achievements:

The project results in a set of 34 outcomes (models, software tools and design flows) including prototypes (22) and exploitable products (12). A set of metrics is available which provides a first evaluation of the benefits of the project.

Time-To-Market: Code synthesis or communication synthesis are accelerated by up to 3 orders of magnitude (depending on case).

Performance: As a first estimation, NEVA improvements amount to:

x1.35 thanks to property aware compiling, x1.35 thanks to re-configurability, x1.6 thanks to optimizations, x3 thanks to ANoC, x8 thanks to frame level parallelisation which gives a (theoretical) total of x70.

At the CAD partners, through an extension of their portfolio of products and/or services or a commercialization of new EDA solutions on the open market.

A huge standardization effort was deployed by the partners of the project, under the leadership of ST, concerning OSCI TLM. These actions highly contributed to the TLM standard 2.0.

2A704: ROBIN

Objective:

While applications require smaller voltages and higher frequencies, miniaturisation adds new risks of voltage distortions. To reduce design iterations and avoid unreliability or failures, ROBIN aims at preventing these effects very soon in the design flow. The project will address signal corruption in Systems-in-Package either at macro-level (power distribution, substrate) or micro-level (interconnect crosstalks, natural radiations). By considering manufacturing constraints, optimal trade-offs will be defined between circuit robustness and efficient use of technology, down to 45 nm.

Project Members:

2A704/C	ROBIN		
ENDED		CISC SEMICONDUCTOR	AT
		CWS	FR
		EDXACT	FR
		HIREX	FR
		INFINEON	AT
		L2MP	FR
		NXP SC	NL
		STMICROELECTRONICS	IT
		STMICROELECTRONICS	FR

Milestones and Resources:

This project was scheduled and executed from 01 January 2005 until 31 December 2008 using 256 PYs.

Status and Achievements:

The project resulted in a set of 53 outcomes consisting of: 33 tools/flows, 18 models/IPs, 2 equipments, 42 productive, 11 prototypes.

These outcomes will benefit to four main types of designers: SoC designers, analog designers, digital designers and back-end designers.

New design flows: Designers not only benefit from an ergonomic progress thanks to integrated flows (see above), but they can also design in a faster way, performing simulations 4 times faster, extractions 30 times faster and pole/zero modelling 100 times faster.

More robust circuits can be designed and built: the bad influence from digital to analog is reduced by 25 dB, circuits can now cope with electrostatic discharges reaching 750 V. This is not done at the expense of consumption: power savings can even reach 40% thanks to new design techniques for on-chip communication.

Money saving: error prevention during SRAM design makes it possible to significantly increase yield during the fabrication of circuits including a large set of such memory blocks.

2A708: LoMoSA+

Objective:

The LoMoSA+ project aims at the creation of a low-power expertise for mobile and multimedia applications by initiating the development of a European low-power System-on-Chip (SoC) platform, consisting of an interacting combination of (architectural) models, design flows and methodologies, hardware design components, embedded software and test-benches.

Project Members:

2A708/B LoMoSA+		
ENDED	DS2	ES
	LETI	FR
	LIST	FR
	NXP SC	NL
	NXP SC	FR
	STMICROELECTRONICS	FR
	THALES COMMUNICATIONS	FR
	THOMSON R&D	FR
	TIMA	FR
	UNI LUGANO - ALARI	CH

Milestones and Resources:

This project was scheduled and executed from 01 January 2005 until 31 December 2008 using 309.7 PYs.

Status and Achievements:

The quantitative target of the LoMoSA project was set to reduce overall system power consumption, i.e. active and standby power, up to 70% by the end of 2008.

- The major technological innovations in LoMoSA concerned;
- Definition of integrated low-power optimised platform architectures,
- Development of a power-aware design methodology and methods,
- Development of reusable, power-efficient digital and analogue HW components that are the building blocks of the platform,
- Development of HdS technology for the application driven design of architectures built on top of NoC (Network-on-Chip) as an enabler of 65 nm technology platforms for European SoC applications,
- Validation of the newly developed technologies was done through a set of jointly developed practical application demonstrators at the end of the project.

At the end of LoMoSA it can be stated that:

Qualitative goals of the project were reached. The quantitative goal of >70% power reduction had to be adjusted. For some LoMoSA results under specific use-cases power reduction comes close or even extends the 70%. In general, the quantitative goal should be: power reduction up to 70%. For a number of demonstrators this quantitative goal has been met.

2A713: HONEY

Objective:

The main goal of HONEY is to allow quick fabrication ramp up to an economically acceptable level. The project intends to address yield and reliability without affecting the silicon process. Circuit compliance with specifications will be extended from fabrication (i.e. yield) to operational circuit life (i.e. reliability). HONEY will propose a consistent yield- and reliability-oriented design flow from block and library levels, down to layout and reticule levels.

Project Members:

2A713/E 2ML2 HONEY		
ACTIVE	DOLPHIN INTEGRATION	FR
	IMEP-LAHC	FR
	IMMS	DE
	INFINEON	DE
	INFINEON	FR
	INFINISCALE	FR
	MUNEDA	DE
	STMICROELECTRONICS	FR
	STMICROELECTRONICS	IT
	X-FAB	DE
	XYALIS	FR

Milestones and Resources:

This project was scheduled to begin on 01 January 2007 and to end on 31 December 2009. Due to funding decisions the project started 01 July 2007 and is scheduled to end 31 December 2010 with the planned resources of 213 PYs.

Status and Achievements:

The year 2009, was aimed at improving the predictions and enhancements from the first phase. A toolbox is available, including models, CAD tools, test structures, flows and methodologies. Current status shows that the solutions proposed by HONEY appear to be very competitive on the market, with in particular: model-based solutions providing a breakthrough in front of slow simulator-based solutions, results of several publications indicating attractiveness of on-line monitors which consider real circuit environment, first mixed mode TCAD simulation of inverter after Soft Breakdown, and yield optimized Pareto front as the first approach able to handle mismatch sensitive performance. Recent quantified improvements are available, concerning design margins, design time, chip area and chip performances.

Exercised applications are mainly those which are highly safety critical (transportation, industry). At least three partners are focusing on Automotive applications. Telecommunication was used as experimentation field, e.g. a 3.5G baseband IC for cellular communication which was used for clock tree analysis (Infineon-G). A new assessment method for library standard cells concerning electromigration was used on 65/40 nm libraries for wireline applications. The Datacom field provided a complex IP named LDPC, used to exercise reliability techniques (ST-F).

2A714: SoftSoC (hardware dependent Software for SoC)

Objective:

SoftSoC started on June 1st 2008. SoftSoC aims at solving the main productivity bottleneck faced by system designers when integrating new IP within existing CPU based platforms. Such integration requires providing HdS to drive the new IP. This HdS is fastidious to develop and very expensive to debug. Moreover, it is also very resource consuming to validate that the new IP work correctly with the rest of the platform. SoftSoC will deliver significant economic value for SoC designers and IP.

The concept is based on a flexible generic architecture made of a fixed computing infrastructure and an extendable part made of Hardware and Software IP that are specific to the application. The SoftSoC project is based on four key innovations to bridge the gap between SoC applications and design methods: IP Modelling breakthrough, IP Integration breakthrough, HdS design automation breakthrough, Standardisation breakthrough.

Project Members:

2A714/D 2ML3 SoftSoC		
ACTIVE	COMPAAN DESIGN	NL
	DS2	ES
	GRASS VALLEY FRANCE	FR
	LETI	FR
	THALES COMMUNICATIONS	FR
	TIMA	FR
	TRIDENT MICROSYSTEMS (NXP SC)	NL
	TU DELFT	NL
	UNI LEIDEN - LIACS	NL
	VIRL	NL

Milestones and Resources:

This project was scheduled from 01 January 2008 until 31 December 2010. Due to funding decisions the start moved to 01 June 2008 and the new planned end date is 31 May 2011. The planned resource usage is 122 PYs.

Status and Achievements:

Thanks to the significant involvement of all partners, the consortium reached consensus on a shared architecture definition of the HDS.

Several tools have been enhanced and the design of the different proof of concepts has commenced.

The most important event of the project in the second semester was the open workshop, which took place in Grenoble during the ESWEEK in October.

The first dissemination activities have been reported.

Very good project as it brings hardware and software together. In order to gain more flexibility in hardware IP selection, the HW/SW design flow is formalised on the HW and low level hardware dependent SW (HdS).

2A717: Beyond Dreams (Design refinement of embedded analogue and mixed-signal systems)

Objective:

Beyond DREAMS will provide methods to handle the complexity and shorten the path from specification to implementation of future analogue mixed signal Systems on Chip / Systems in Packages / Hardware / Software and in heterogeneous systems (mechanical, optical, etc.). Extensions for AMS modelling and simulation will be issued in the SoC domain standards: SystemC and IP-XACT via the Standardization bodies OSCI and ACCELLERA. Demonstrators based on industrial test cases will be developed.

Project Members:

2A717/C 2ML3 Beyond Dreams		
ACTIVE	DIZAN-SYNC	NL
	FHG IIS - EAS	DE
	IMEC STICHTING	NL
	INFINEON	DE
	LETI	FR
	LIP6	FR
	MDS	FR
	ROBERT BOSCH	DE
	STMICROELECTRONICS	FR
	TIMA	FR
	TRIDENT MICROSYSTEMS (NXP SC)	NL
	TU DELFT	NL
	UNI VIENNA-ICT	AT
	WMC	NL

Milestones and Resources:

This project was scheduled from 01 January 008 until 31 December 2010. Due to funding decisions the start moved to 01 October 2008 and the new planned end date is 30 September 2011. The planned resource usage is 94 PYs.

Status and Achievements:

During 2009 papers were submitted and presentations were made. The current project progress is in line with the schedule.

The first SystemC-AMS course has been started at the UPMC University in the frame of a Master Diploma, with a strong success.

The Beyond DREAMS partners are working in close cooperation with German SyEnA partners on the definition of a simulatable specification.

During this same period papers and presentations were made during DAC 2009, FDL'09, ECCTD'09 , PATMOS, IEEE-SOCC 2009, plus posters and demonstrations during the MEDEA+/CATRENE forum in Noordwijk.

The main standardization effort was to consolidate all community feedback of the SystemC AMS extensions Language Reference Manual update and to start the development of a user's guide. In parallel, the new modelling standard and its concept have been presented at conferences and workshops.

2A718: TSAR (Tera-Scale multi-core processor ARchitecture)

Objective:

The TSAR project proposes to explore MPSoC computing architectures both at hardware and software levels to support parallelism for which purpose cache coherence and memory consistency management by hardware may bring flexibility to the definition and execution of parallel tasks. Trade-off between performance and correctness in parallel programming is thus resolved through configurable architectures supporting a wide range of memory models to implement a large spectrum of lock grain.

Therefore, the key targets of TSAR are: To investigate innovative hardware design including In-Network cache coherence protocol design, application specific NoC Design and software development targeting optimal multi-core compilation for a wide range of memory models (streaming and cache coherence models); To design configurable NoC-based multi-core architectures supporting a range of memory models and particularly an In-Network cache coherence protocol; To adapt and optimize software compilation to such configurable multi-core architectures (e.g. automatic parallelization of C program into KPN); To demonstrate the proof of concept on virtual prototypes and hardware FPGA-based platforms.

The ultimate goal of TSAR is to provide high-performance and scalable multi-core (virtual and FPGA-based) platforms to attract the industrial communities to develop applications on them.

Project Members:

2A718/B 2ML3 TSAR		
ACTIVE	ACE	NL
	BULL	FR
	COMPAAN DESIGN	NL
	LETI	FR
	LIP6	FR
	PHILIPS HEALTHCARE	NL
	THALES COMMUNICATIONS	FR
	TRIDENT MICROSYSTEMS (NXP SC)	NL
	TU DELFT	NL
	UNI LEIDEN - LIACS	NL

Milestones and Resources:

This project was scheduled from 01 April 2008 until 31 December 2010. Due to funding decisions the start moved to 01 June 2008 and the new planned end date is 30 May 2011. The planned resource usage is 86 PYs.

Status and Achievements:

During the reporting period, progress of the TSAR project is consistent and coherent with the project schedule as defined in the last Full Proposal. In addition to these internal activities, the TSAR consortium also made an effort to open the project to the outside world.

Activities around industrial exploitation and dissemination are ongoing.

3. CATRENE PROJECTS IN TECHNOLOGIES

CT105: 3DIM3 (CATRENE 1ST CALL PROJECT)

Objective:

The project aims at providing novel system methodologies, new design tools and system architecture solutions to handle emerging 3D integration technologies for multimedia and mobile (M3) product. Therefore, the 3DIM3 project will enable the design, from system and architecture level to layout, of 3D integrated M3 products with higher performances, lower consumption, and smaller size/form factor at lowest cost.

Project members:

CT105/A	CL1	3DIM3	
ACTIVE		CADENCE DESIGN SYSTEMS	FR
		EADS SN	FR
		FHG IIS - EAS	DE
		INFINEON	DE
		INL - ECL	FR
		LETI	FR
		NXP SC	FR
		R3LOGIC	FR
		RECORE SYSTEMS	NL
		STMICROELECTRONICS	FR
		TIMA	FR
		TRIDENT MICROSYSTEMS (NXP SC)	NL
		TU DELFT	NL
		VIRAGE LOGIC	NL

Dates and Resources:

This project was scheduled to begin in January 1st 2009 and actually began in July 1st 2009 and is scheduled to end in June 3Oth 2012. The original project lifetime on 36 months is on schedule to be met. Total manpower: 277 P.Y

Status and Achievements:

The first Project Review was done on June 3 2010 in Grenoble. Most of the tasks started as planned excepted when German partners are involved, in that case they are frozen waiting for inputs from the German consortium. The new delay of German partners is now hampering the whole project.

Nevertheless first significant results in all Work Packages are very encouraging.

CT204: PASTEUR (CATRENE 1st Call Project)

Objective:

This project aims at exploring and developing RFID-based sensor platform technology, which will be demonstrated in an intelligent package monitoring the environmental conditions of perishable goods in the supply chain between production and consumer and therefore guaranteeing a more effectively product's quality. The PASTEUR project thereby addresses the need to increase on-line knowledge on the traceability of individual products and the demand to increase the accessibility of the information about these products for the consumer end-user. Key differentiators in the technologies to be developed are ultra-low power and extreme low cost.

Project members:

CT204/1	CL1	PASTEUR	
ACTIVE		BOSCHMAN TECHNOLOGIES	NL
		DSM	NL
		HOLST CENTRE / TNO	NL
		IMB - CNM	ES
		IMEC STICHTING	NL
		INKOA	ES
		KUL - ESAT	BE
		NTC WEIZ GMBH	AT
		NVC	NL
		NXP SC	AT
		NXP SC	BE
		NXP SC	NL
		PHILIPS APPLIED TECHNOLOGIES	NL
		PHILIPS CL	NL
		PHILIPS MIPLAZA	NL
		PRELONIC	AT
		TU DELFT	NL
		TU EINDHOVEN	NL
		VERHAERT	BE
		WUR	NL

Dates and Resources:

This project has begun as planned in July 1st 2009 and is scheduled to end in June 30th 2012. The original project lifetime on 36 months is on schedule to be met.
Total manpower: 146 P.Y

Status and Achievements:

The status concerning the funding in the different countries has been cleared out in S2-2009. Four countries approved the funding for the Pasteur project, while Germany decided not to fund the project. The Netherlands, Belgium, Austria and Spain are the four countries. The impact of the declined funding in Germany and the reduced funding in Belgium versus the Full Proposal has quite a significant impact on the work plan, since all partners decided to withdraw all non-funded tasks from the project but this will not compromise the overall aims of the project.

All changes have been submitted and accepted on February 2010 in a major change request.
The biggest impact of the funding reduction is mainly on WP1 but other impacts on WP2, WP4 and WP5 are visible. First results are promising.

CT205: REFINED (CATRENE 2ND CALL PROJECT)

Objective:

The REFINED project aims to create fully integrated technology platforms for the embedding of NVM functions in sub-90 nm CMOS technologies (process, demonstrator, and test and reliability infrastructure) and in parallel to setup low cost effective solutions for qualified technologies.

It brings together the main European R&D actors (semiconductor companies, research laboratories), to develop the 65 nm generation as well as improvements to the current 90 nm generation (shrink version). The base for the next generation is also set along evolutionary approaches as well as more radical ones. Essential issues of reliability, testing and IP development are addressed in parallel. The REFINED project ensures the continuation of Europe leadership in the field of embedded non volatile memories.

Project members:

CT205/1	CL2	REFINED	
ACTIVE		ATMEL ROUSSET	FR
		INFINEON	DE
		LETI	FR
		STMICROELECTRONICS	FR
		STMICROELECTRONICS	IT
		ST ROUSSET	FR

Dates and Resources:

This project begins as planned in January 1st 2010 and actually began in July 1st 2009 and is scheduled to end in December 31st 2012. The original project lifetime on 36 months is on schedule to be met.

Total manpower: 200 P.Y

Status and Achievements:

The project started January 1st 2010 despite unclear funding situation in Italy and some delay to obtain funding in France and Germany.

The funding situation is still unclear for Italy. For Germany (Saxony), the funding is agreed till March 2011. The German partners will have a new negotiation for the remaining period of the project.

Even if there will be probably no funding in Italy in 2010, ST-Agrate will maintain his effort in areas where there is direct dependence of deliverables with the other partners in order not to jeopardize the overall program progress. A change request taking into account all the following changes has been submitted and accepted in June 2010:

- 3 partners (NXP, IMEC, TUDelft) withdrew from the project and tasks planned for these partners removed from the project.
- Refocus of ST eFlash technology from 65 nm to 55 nm
- Update work plan according to the remaining participants (Partial integration of WP4 into WP3 to keep a full work plan consistent)

All milestones planned for the first half of 2010 have been met and the milestones for the next period (H2 2010) are announced to be “on track.”

CT206: UTTERMOST (CATRENE 2ND CALL PROJECT)

Objective:

The main goal of the UTTERMOST project is to develop advanced process modules, and validate a design platform (design kit, models, and libraries) for reliable and manufacturable digital CMOS 32/28 nm technologies on 300 mm wafers. For the first time, 3 European companies, member of the IBM R&D ALLIANCE "ISDA" will collaborate to develop the latest core digital CMOS Technology Platform and deploy the technology at design and manufacturing level in parallel. Additionally Numonyx (NMX) will develop a 32 nm technology platform dedicated to memory applications more specifically Non Volatile Memories (NVM). By targeting an extra half node beyond the 32 nm, the UTTERMOST project, has the ambition to promote Europe at the forefront of the semiconductor industry.

Project members:

CT206/1	CL2	UTTERMOST	
ACTIVE		ALCATEL-LUCENT	DE
		AMIL	IL
		CAMECA	FR
		CARL ZEISS SMT	DE
		CEMES	FR
		DOLPHIN INTEGRATION	FR
		FHG IIS - EAS	DE
		FHG IISB	DE
		FHG-IZFP	DE
		GF	DE
		IBS	FR
		IMEP	FR
		INFINEON	DE
		INFINEON	FR
		IPGEN	DE
		LAM RESEARCH	FR
		LAM S.R.L.	IT
		LETI	FR
		LETI/INAC	FR
		LTM	FR
		NOVELLUS S.R.L.	IT
		NOVELLUS SYSTEMS	FR
		NUMONYX	IT
		SERMA TECHNOLOGIES	FR
		ST-ERICSSON	FR
		STMICROELECTRONICS	FR
		TEL	IT
		THALES COMMUNICATIONS	FR
		UNI STUTTGART	DE

Dates and Resources:

This project was scheduled to begin in January 1st 2010 and actually began in June 1st 2010 and is scheduled to end in June 30th 2013. The original project lifetime on 36 months is on schedule to be met. Total manpower: 551 PY

Status and Achievements:

The status concerning the funding in the different countries has been cleared out in June 2010. The project start date is June 1st 2010 but not for the full consortium: France has issued contracts to 13 out of 15 French partners. Germany has issued contracts to 5 out of 9 German partners and the other partners including GF will join at a later date. The whole Italian consortium has cancelled its participation (no funding) The partner from Israel was associated to a German partner whose activity was non funded hence will not participate either. The changes in the consortium perimeter from 32 to 21 partners as well as power reductions for some of the remaining partners will be detailed in a Change Request to be issued in September 2010.

CT207: COCOA (CATRENE 2nd Call Project)

Objective:

This project aims at developing a complete mature 3D integration technology platform covering the entire range of processes required from vertical interconnects (TSV, micro bumps...) and robust bonding to innovative packaging approaches to address a wide range of products. The main objectives of this project is to achieve chip-level three-dimensional (3D) TSVintegration, Wafer-to-Wafer and Die-to-Wafer bonding, and packaging of stacked circuits, in order to create a complete technological platform for high performance and cost effective 3D systems manufacturing. The objective of COCOA project is to define a robust 3D integration technology platform covering the existing gap between medium (104 cm^{-2}) and high density (106 cm^{-2}) technologies, including packaging of two or more stacked layers.

Project members:

CT207/1	CL2	COCOA	
ACTIVE		ALSI	NL
		ASM	NL
		ASM BELGIUM	BE
		AUSTRIAMYCROSYSTEMS	AT
		BOSCHMAN TECHNOLOGIES	NL
		DATACON	AT
		EVG	AT
		FHWN	AT
		IM2NP	FR
		LAM RESEARCH	FR
		LETI	FR
		SEIBERSDORF RESEARCH	AT
		SEMITOOL	FR
		ST-ERICSSON	FR
		ST TOURS	FR
		STMICROELECTRONICS	FR
		STS	UK
		TNO - SCIENCE AND INDUSTRY	NL
		TRIDENT MICROSYSTEMS (NXP SC)	NL
		TU DELFT	NL
		UNI VIENNA / EMST	AT

Dates and Resources:

This project begin was scheduled to begin in January 1st 2010 and actually began in July 1st 2010 and is scheduled to end in June 30th 2013. The original project lifetime on 36 months is on schedule to be met.
Total manpower: 176 PY

Status and Achievements:

The project start date is July 1st 2010 with a modified consortium. French and Austrian partners have been able to start activities and one partner from Belgium (ASM) has started without funding.
A Change Request is planned to be issued in September 2010 to take into account the withdrawal of several partners due to lack of funding.

CT301: EXEPT (CATRENE 1st Call Project)

Objective:

The goal of the EXEPT project is to develop technologies, tools & infrastructures components as required for high volume EUV lithography for 22 nm node in 2012. The project aims with the expected introduction of EUV lithography in high volume semiconductor production lines at opening new business opportunities for the participating companies, at positioning the institutes at prominent levels in their fields of activities and overall at safeguarding the international semiconductor industry in enabling the realization of their technology roadmap in lithography as given in the ITRS.

Project members:

CT301/B	CL1	EXEPT	
ACTIVE		ALCATEL VAC. TECH.	FR
		AMTC	DE
		ASM BELGIUM	BE
		ASML	NL
		BRUKER AXS	DE
		CARL ZEISS SMT	DE
		DMS	DE
		FHG IIS	DE
		FOM - RIJNHUIZEN	NL
		HAMA TECH APE	DE
		IMEC	BE
		IMS CHIPS	DE
		MEDIA LARIO	IT
		NAWOTEC	DE
		PHILIPS EUV	DE
		SAGEM DEFENSE SECURITE	FR
		XENOCS	FR
		XTREMETEC	DE

Dates and Resources:

This project has begun as planned in February 1st 2009 and is scheduled to end in March 31st 2012. The original project lifetime on 36 months is on schedule to be met.
Total manpower: 1328 PY EXEPT is the largest MEDEA+/CATRENE project.

Status and Achievements:

The second Project Review is scheduled on December 9th 2010.

Five countries (Belgium, France, Italy, Germany and The Netherlands) and 15 partners are involved. Germany and The Netherlands, represent 87% of the total manpower. Italian partner (Media Lario) is participating without funding. The funding situation granted for the first year has not been clearer yet. The final funding approbation for the total project duration will depend of the pending positive result notification in Brussels. In the reporting period good progress have been made in all work packages and clear recovery plans put in place in H1-2010 allowed to complete most of the tasks with a maximum shift of 1 quarter versus the initial schedule. The consequences of delays on tasks of other work package and project realization are anticipated and minimized.

CT302: TOETS (CATRENE 1st Call Project)

Objective:

The TOETS project has the ambition to create a breakthrough in methods and flows used by the test technologies by considering test in the whole value chain from Design to Application. The ongoing evolution in microelectronics allows the semiconductor industry to create nanoscale devices in combination with gigascale complexity.

A strong consortium composed of European Semiconductor industries, Academics and SMEs has grouped their competences to successfully address this challenge. Test is becoming a dominant factor in overall manufacturing cost. Furthermore, the semiconductor industry is extremely competitive and is asking for the best quality and reliability levels at the lowest cost.

Project members:

CT302/A	CL1	TOETS	
ACTIVE		ADD	ES
		ATMEL NANTES	FR
		D4T SYSTEMS	NL
		E2V SEMICONDUCTORS	FR
		IMSE - CNM	ES
		INESC PORTO	PT
		INFINEON	AT
		INFINEON	FR
		IROC TECHNOLOGIES	FR
		JTAG TECHNOLOGIES	NL
		KUL - ESAT	BE
		LETI	FR
		LIRMM	FR
		LIST	FR
		NXP SC	FR
		OPHTIMALIA	FR
		PHILIPS HANDSHAKE SOLUTIONS	NL
		QSTAR TEST	BE
		SALLAND ENGINEERING	NL
		STMICROELECTRONICS	FR
		SUPELEC	FR
		TEMENTO SYSTEMS	FR
		TIMA	FR
		TOMORROW OPTIONS	PT
		TRIDENT MICROSYSTEMS (NXP SC)	NL
		UNI TWENTE	NL

Dates and Resources:

This project has begun as planned in March 1st 2009 and is scheduled to end in March 31st 2012. The original project lifetime on 36 months is on schedule to be met.
Total manpower: 304 PY EXEPT is the largest MEDEA+/CATRENE project.

Status and Achievements:

The project started on March1st, 2009 with the partners from Austria, France, Portugal and The Netherlands. The funding for the 2 remaining countries Belgium and Spain is not yet granted. Due to non-funding of the Belgian partner (Q-Star) and Spanish partners (ADD, IMSE-CNM) in 2009, some tasks could not be started yet or have minor progress. Nevertheless all scheduled milestones for the reporting period have been reached. The second Project Review is scheduled on October 7th, 2010.

4. CATRENE PROJECTS IN APPLICATIONS

CA101: PANAMA

Objective:

The PANAMA project objective is to improve the efficiency of each power amplification stage for multimode multistandard applications, by taking into account overall transmit and receive chains and more capability for each applications, spectral efficiency improvement. The results of the project in terms of integrated PAs (SiP and SoC) as well as the discrete PA (BTS, Avionics and Satcom), the developed methodologies and tools will be used by the European microelectronics and system providers to make a breakthrough in the wireless market and then to increase their competitiveness.

Main common target is an efficiency gain for each application:

- 20% compared for integrated systems,
- 30% for discrete systems,
- 10% for distributed systems.

Beyond the realisation of these PA systems, PANAMA relies on the development of innovative enabling tools in measurements, modelling and simulation areas allowing breakthrough in the design flow.

Project Members:

CA101/B	CL1	PANAMA	
ACTIVE		AGILENT	BE
		AMCAD	FR
		ESIEE PARIS	FR
		GIGLE SEMICONDUCTOR	ES
		IEMN	FR
		ELTA SYSTEMS	IL
		IMS LAB	FR
		INSTITUTE TELECOM	FR
		KUL-ESAT	BE
		LETI	FR
		MC2 TECHNOLOGIES	FR
		NXP SC	FR
		OMP	BE
		ST-ERICSSON	BE
		STMICROELECTRONICS	FR
		THALES COMMUNICATIONS	FR
		TNO DSS	NL
		TRIDENT MICROSYSTEMS (NXP SC)	NL
		TU DELFT	NL
		TU EINDHOVEN	NL
		UPC	ES

Milestones and Resources:

This project was scheduled from 01 October 2008 until 31 December 2011. Due to funding decisions and lack of resources of some partners the start moved to 01-01-2009 and the new planned end date is 30 September 2011. The planned resource usage is 202 PYs.

Status and Achievements:

All Public Authorities had approved the budget. The project is managed well. After last year focus on technology, process and architecture choices, the main activities have been on design and on non linear characterization tools.

CA103: HERTZ

Objective:

The objective of the HERTZ project is to enable energy savings in homes of consumers by providing home energy control systems. This requires three elements;

- Notion of context, based on sensors,
- Control of equipment that consume energy, such as lighting and brown goods,
- Connectivity between sensors and equipment, realized through a wireless infrastructure.

Obviously, all three elements of the home energy control system must be energy efficient themselves too, this is however not straightforward to achieve.

Project Members:

CA103/C	CL1	HERTZ	
ACTIVE		DICE	AT
		DS2	ES
		INFINEON	AT
		IQUADRAT	ES
		LANTIQ	AT
		PHILIPS APPLIED TECHNOLOGIES	NL
		PHILIPS CL	NL
		PHILIPS LIGHTING	NL
		QUINTOR	NL
		SITEL	NL

Milestones and Resources:

This project was scheduled from 01 July 2009 until 30 June 2012. Due to funding decisions and lack of resources of some partners the start moved to 01 October 2009 and the new planned end date is 30 September 2012. The planned resource usage is reduced from 257 to 127 PYs.

Status and Achievements:

The project is on track and the major achievements of this reporting period are, that the Use Case scenarios were agreed, the G.hn standard approved and a tape out of the low power wireless transceiver test chip was produced. A big step towards the goals of the HERTZ project was the publication of the RF4CE (radio frequency for consumer electronics) protocol which represents the demanded low power consuming wireless network technology.

The project will enable the consortium partners to secure a leading position in the emerging domain of ambient intelligence. The results will have a direct impact on the future way of living of citizens in Europe and worldwide. This has been described in the paragraphs on “Exploitation” and on “Relevance for Europe,” respectively. Beyond this direct impact, the project will enhance academic and industrial research and development in the general domain of wireless sensor networks and associated application fields.

CA104: COBRA

Objective:

Replace Heterogeneous mixed HW/SW specialized sub-systems by a single scalable and programmable computing fabric while solving manufacturability issues.

Hardwired SoC architectures suffer from a lack of flexibility regarding market evolution, resulting in an excessive design cycle time and increased cost. Furthermore, process variability is not yet well addressed for 32 nm and beyond. The objective of COBRA is to develop and experiment an open, flexible and high performance platform by substituting heterogeneous hardware/software subsystems by a regular array of processors combined with asynchronous architectures to be used to design COBRA clusters of processors, which are "globally asynchronous." The platform will be driven by Telecom, Video and Multimedia benchmark applications and demonstrated on 32nm silicon with 3D stacking.

Project Members:

CA104/A	CL2	COBRA	
ACTIVE		ACE	NL
		CAPS ENTREPRISE	FR
		COMPAAN DESIGN	NL
		ECOMUNICAT	ES
		DS2	ES
		LETI	FR
		LIST	FR
		SAPEC	ES
		ST-ERICSSON	NL
		STMICROELECTRONICS	FR
		TEDESYS	ES
		TRIDENT MICROSYSTEMS (NXP SC)	NL
		TU DELFT	NL
		TU EINDHOVEN	NL
		UAB	ES
		UNI CANTABRIA	ES
		VIRAGE-LOGIC	NL
		VISTA-SILICON	ES

Milestones and Resources:

Since the labelling of the project (FP V2, Nov.2009), and due to funding constraints, a set of changes occurred in COBRA. The Dutch partners extending their works by 4 months (new ending date: 30 April 2013). The funding situation: positive in France and Spain; funding approval in The Netherlands.
The planned resource is 267 PYs.

Status and Achievements:

The project started on January 1st, 2010 in two countries. The project is preceding in-line with FP V3.

CA201: TS-CIMoNHet

Objective:

The TS-CIMoNHet project (Trust and Security in Critical Infrastructure, Mobile Networks & Heterogeneous Networked Environments) aims at developing a family of HW/embedded SW silicon components together with their management procedures for ensuring and re-enforcing Privacy, Trust and Security of transactions in some public critical infrastructures as well as in high value ambient-intelligence scenarios pertaining to the emergence of the future "Internet of Things" and linked to "Machine to machine" or "man to machine" interactions.

The TS-CIMoNHet project will capitalize on some of the results developed in the MEDEA+ TSC project.

Project Members:

CA201/A	CL2	TS-CIMoNHet	
ACTIVE		APPLUS+	ES
		BERTIN TECHNOLOGIES	FR
		BIOACCEZ CONTROL	ES
		EADS DS	FR
		ENSM	FR
		ESI	ES
		FRANCE TELECOM R&D	FR
		GEMALTO	FR
		GREYC	FR
		INSTITUTE OF TECHNOLOGY	IE
		INSTRINSIC ID	NL
		SOLAIEMES	ES
		STMICROELECTRONICS	FR
		TB SOLUTIONS	ES
		TECHNIKON	AT
		UNI CANTABRIA	ES
		UNIVERSITY COLLEGE CORK	IE
		UNIVERSITY REY JUAN CARLOS	ES

Milestones and Resources:

This project was scheduled from 01 January 2010 until 31 December 2012. The planned resources are 185 PYs.

Status and Achievements:

This project has yet to start.

The project will key Sovereignty, Protection against fraud, Daily life of citizens, Importance for European economy.

By creating a critical mass on the subject, the project will be able to bring sound contributions to all related standardization initiatives (TCG, IETF, ETSI , OMA).

CA202: eGo

Objective:

This project aims at developing new HW and embedded SW devices that will fully comply with the next wave of computing and will fully integrate in both "ambient-intelligence" and "internet of things" scenarios. More precisely, the project will develop, prototype and experiment with new ways of establishing high-speed, secure bidirectional wireless communication channels and supporting new, intuitive and simple context-sensitive interactions between persons and objects belonging in the environment. Furthermore, these interactions will by necessity preserve both the security and privacy of the transactions.

More precisely the project will develop new types of devices (named eGo and eGo compliant devices) that will integrate very low-power MEMS or sensors together with secure embedded electronics that will enable immediate "Touch and use" interaction between persons and objects.

Project Members:

CA202/A	CL2	eGo	
ACTIVE		ATOS WORLDLINE	FR
		CIE	FI
		CONTINENTAL	FR
		DECAWAVE	IE
		GEMALTO	FR
		IDEX	NO
		INRIA	FR
		INSTITUTE OF TECHNOLOGY	IE
		LINCOR SOLUTIONS	IE
		PRECISE BIOMETRICS	SE
		STMICROELECTRONICS	FR
		TYNDALL INSTITUTE	IE
		VTT	FI
		YOUGETITBACK	IE

Milestones and Resources:

This project was scheduled from 01 January 2010 until 31 December 2012. The planned resource usage is 146 PYs. This project started 1st of July 2011.

Status and Achievements:

This project is in start-up phase.

The fundamental activities on 3D thin film batteries, inertial and biometric sensors will enable a wide range of new applications and products. The single components and their combination play an important role for the ubiquitous electronics and their required context awareness.

CA301: HiDRaLoN

Objective:

The objective of HiDRaLoN is to address societal needs in the areas of healthcare, entertainment, and road & industrial safety. This project will lead to a number of societal benefits: higher efficiency, less errors in medical diagnostics, change from treatment to prevention, enhanced experience for TV viewers by unprecedented image quality, an additional pair of "automatic" eyes on the road, see more in a dark environment, improved recognition capabilities, improved safety and flexibility of assembly lines to safeguarding man and machine.

Of the many performance aspects of a CMOS imager HiDRaLoN will focus on increasing the dynamic range to 120dB and lowering the noise level with at least 50% to make CMOS imagers surpass today's CCDs. Obviously best practices known from CCD manufacturing will be maintained.

The project will deliver five new imagers for the 3D imaging, Medical, Broadcast, and Safety/Security/ Machine Vision markets, and algorithms to correct flaws of the imagers and the optics. Demonstrations in the project will focus on general purpose imaging, medical and broadcast applications.

Project Members:

CA301/D	CL1	HiDRaLoN	
ACTIVE		CRS	DE
		E2V SEMICONDUCTORS	FR
		FHG IMS	DE
		GRASS VALLEY NEDERLAND	NL
		HELION	DE
		IMS CHIPS	DE
		LE2I	FR
		NIKHEF	NL
		ORBOTECH MS	IL
		PHILIPS HEALTHCARE	IL
		PHILIPS HEALTHCARE	NL
		PHILIPS RESEARCH	DE
		PILZ	DE
		THALES ANGENIEUX	FR
		TU DELFT	NL
		UNI BUDAPEST	HU
		VIIMAGIC	DE
		VIKING	HU

Milestones and Resources:

This project was scheduled from 01 January 2009 until 31 December 2011. Due to funding decisions and changes of legal entities of some partners the start moved to 01 March 2009 and the new planned end date is 30 June 2012. The planned resource usage is 247 PYs.

Status and Achievements:

In the first half of 2010 in total 10 deliverables have been created of which 2 have slipped into July.

CA303: OPTIMISE

Objective:

This project aims at developing optimised mitigations for advanced digital and power electronic systems in order to solve the major issue of their reliability against the increasing problem of soft, firm and hard errors.

To reach this goal, end-users, semiconductor manufacturers are associated with technology developers and European academic partners.

The expected deliverables are a set of validated mitigation techniques from layout to applications architecture levels, customised mitigations for given applications and a strong effort in standardisation.

The expected benefits will be the capability to use advanced electronics in critical end-user applications, and ensure reliability of consumer electronic, especially for low power.

Project Members:

CA303/D	CL1	OPTIMISE	
ACTIVE		AIRBUS	FR
		ALTER	ES
		ARQUIMEA	ES
		ATMEL NANTES	FR
		CEA-DAM	FR
		CONTINENTAL	FR
		D&T MICROELECTRONICA	ES
		EADS IW	FR
		IMB-CNM	ES
		IM2NP	FR
		IMS LAB	FR
		IROC TECHNOLOGIES	FR
		RENAULT	FR
		ST ROUSSET	FR
		ST TOURS	FR
		TIMA	FR
		UC3M	ES
		UIB	ES
		VALEO INTERIOR CONTROLS	FR

Milestones and Resources:

This project was scheduled from 01 April 2009 until 31 March 2012. Due to funding decisions the start moved to 01 July 2009 and the new planned end date is 30 June 2013. The planned resource usage is 155 PYs.

Status and Achievements:

All the work packages have started technical works. Specification of digital and power applications to be used all along the project is finished. Partners have identified several mitigation techniques, and are already working on their optimization and validation. Validation plans are under discussion. Standardisation effort and dissemination are already in progress, several initiatives have been initiated.

CA402: THOR

Objective:

This project aims at developing highly efficient, integrated and reliable power electronics technologies for automotive, aeronautics and healthcare applications. The project covers the development of new technologies for discrete power components, power cores, storage elements, packaging for high temperature, thermal and EMC management solutions. The expected deliverables are reliability design oriented prototypes of: Miniaturized high voltage (200V to 3000V), high frequency and high temperature power modules based on new wide band gap semiconductors (SiC or GaN), advanced IGBT's / Si-diodes and high temperature SOI or SiC drivers, and DC/DC converters using improved Si based IGBTs. The expected benefits will be the availability in Europe of such technologies, from power electronics components to complete systems.

Project Members:

CA402/C	CL2	THOR	
ACTIVE		AMPERE LABS	FR
		BARCELONA SEMICONDUCTORS	ES
		BATSCAP	FR
		BRUCO	NL
		CIRTEM	FR
		CISSOID	BE
		EADS IW	FR
		EHP	BE
		EPSILON	FR
		HCM	FR
		HISPANO-SUIZA	FR
		IMB - CNM	ES
		MITRA INNOVATIONS	BE
		NXP SC	BE
		PHILIPS APPLIED TECHNOLOGIES	NL
		PHILIPS HEALTHCARE	NL
		PRODRIVE	NL
		SOITEC	FR
		ST TOURS	FR
		ST-F AUTOMOTIVE	FR
		TRIDENT MICROSYSTEMS (NXP SC)	NL
		TPC	FR
		TU DELFT	NL
		TU EINDHOVEN	NL
		UCL	BE
		UNIVERSITY OF VERSAILLES-SAINT-QUENTIN-EN-YVELINES	FR
		VALEO VEES	FR

Milestones and Resources:

This project was scheduled from 01 January 2010 until 03 September 2013. The planned resource usage is 342 PYs. This project started 1st of October 2010.

Status and Achievements:

This project is in start-up phase.

CA501: COMCAS

Objective:

This project "COMCAS" aims at breakthrough low-power design solutions for (data) communication-centric heterogeneous multi core architectures targeting 45nm and 32nm CMOS technologies. These architectures will be exploited in a number of future applications e.g. the next generation of programmable multi-processor mobile phones and mobile digital entertainment devices. COMCAS investigations concern the complete low-power design hierarchy looking at all aspects from system level choices, modelling of applications (algorithms, protocols) and architectures, maximize the reuse of existing IPs using the most appropriate tool chains, partitioning and mapping, cycle-accurate and bit-true virtual prototyping, minimal power design blending semi- and full custom circuit designs at transistor level in technologies of 45 nm and beyond.

Project Members:

CA501/D	CL1	COMCAS	
ACTIVE		ATRENTA	FR
		AXIOM IC	NL
		DS2	ES
		LEAT	FR
		LETI	FR
		LIST	FR
		RECORE SYSTEMS	NL
		SAYME	ES
		ST-ERICSSON SOPHIA	FR
		ST-ERICSSON	NL
		STMICROELECTRONICS	FR
		THALES COMMUNICATIONS	FR
		TIMA	FR
		TRIDENT MICROSYSTEMS (NXP SC)	NL
		TU DELFT	NL
		TU VALENCIA	ES
		UCLM	ES
		VIRAGE LOGIC	NL

Milestones and Resources:

This project was scheduled from 01 January 2009 until 31 December 2011. Due to funding decisions the start moved to 01 March 2009 and the new planned end date is 29 February 2012. The planned resource usage is 289 PYs.

Status and Achievements:

COMCAS project progressed well in the beginning of 2010.
The fully integration of the new partners and the new teams resulted in a delay of the milestones M1b and M16. A project website has been created. The public website www.comcas.eu provides anybody with interest in the project information.
The project will open new business opportunities thanks to the openness of the system compared to the today close system with the support of applications which have not been foreseen when the product was launched.

CA502: SEEL

Objective:

The goal of the SEEL project is to develop energy efficient and dynamic lighting systems based on HID and SSL for general lighting and automotive lighting, in specific for the professional market. The focus point of the project is the upcoming availability of smart and energy efficient electronics, which is seen as the key enabler to realize the desired performance improvement. Use of intelligent driving schemes and integration of components, to realize miniaturization at low cost, is the way to go. Beside this, standardization will be part of the project in order to enable high volume applications. This also enables cost reduction for the light sources next to securing a leading position for the European Lighting industry now and in the future.

Project Members:

CA502/C	CL2	SEEL	
ACTIVE		ANTARES ILUMINACION	ES
		AUDI	DE
		B+W	DE
		BAG ELECTRONICS	DE
		BESI-FICO	NL
		BIC INDUSTRIES	NL
		BJB	DE
		DCD TECHNOLOGY	NL
		ELMOS	DE
		FHG IZM	DE
		IBERLED	ES
		INFINEON	DE
		INVERTO	BE
		LEITAT	ES
		LETI	FR
		MODULAR LIGHTING	BE
		NXP SC	DE
		OSRAM	DE
		PHILIPS AUTOMOTIVE LIGHTING	DE
		PHILIPS INNOVATIVE APPLICATIONS	BE
		PHILIPS LIGHTING	NL
		PHILIPS RESEARCH	NL
		PHPL	FR
		RUHR - UNI BOCHUM	DE
		STMICROELECTRONICS	NL
		TRIDENT MICROSYSTEMS (NXP SC)	NL
		TU DELFT	NL
		TU EINDHOVEN	NL
		VALEO VISION	FR
		VITO	BE

Milestones and Resources:

This project was scheduled from 01 September 2010 until 31 August 2013. The planned resource usage is 278 PYs.

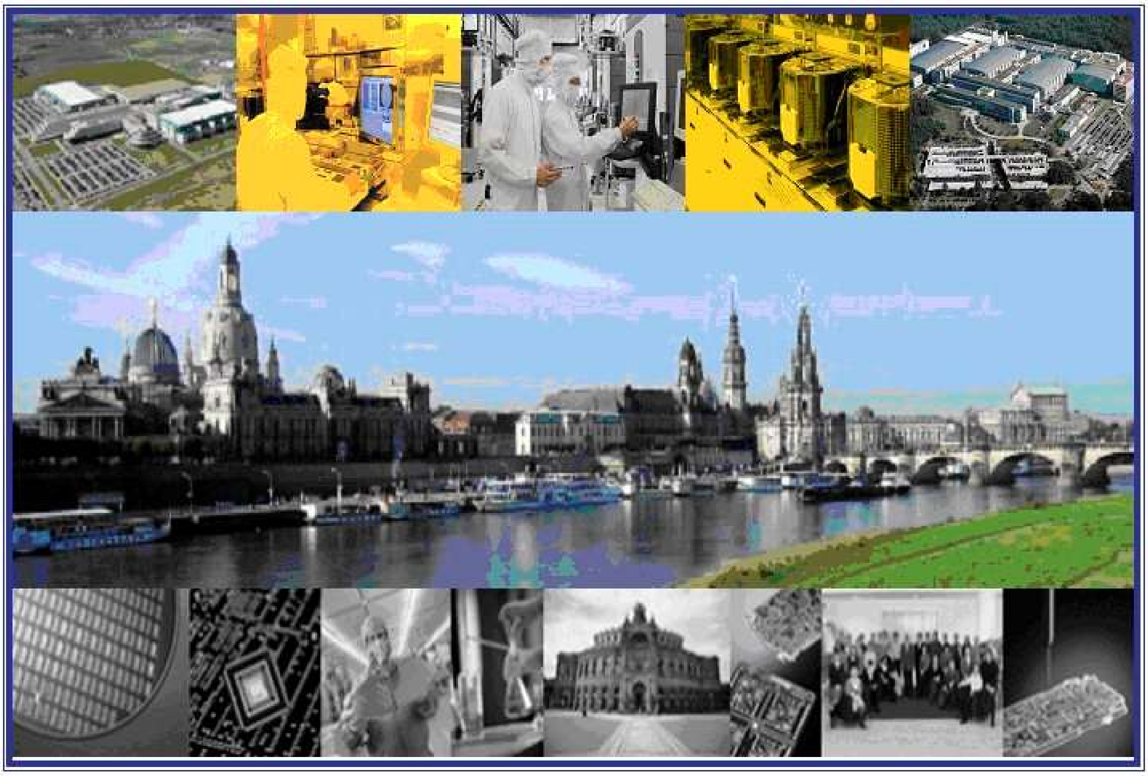
Status and Achievements:

This project is in start-up phase. The most relevant exploitation of the results of this project will be the launch of new products.

ANNEX B: A REVIEW OF THE CATRENE R&D INITIATIVE IN NANOELECTRONICS, FUTURE HORIZONS REPORT

FUTURE HORIZONS
Presents

A Review of the CATRENE R&D Initiative In Nanoelectronics



November 2010

A Focused Industry Report From Europe's Leading Semiconductor Industry Analyst

Future Horizons

A Review of the CATRENE R&D Initiative In Nanoelectronics

November 2010

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Introduction

This Report summarises the results of Future Horizons' October 2010 independent expert audit of the CATRENE office MEDEA+ Phase 2 and CATRENE Programmes Assessment Report.

For the past two decades, the EUREKA JESSI (1989–1996), MEDEA (1997-2000), and MEDEA+ (2001-2008) programmes have made it possible for Europe's industry to reinforce its position in semiconductor process technology, manufacturing and applications, and in so doing to become a key supplier to key world markets such as telecommunications, consumer and automotive electronics, whereby European industry has today successfully:

- Conquered vital high technology domains through technical innovation;
- Learned horizontal and vertical co-operation; and
- Produced several globally successful industrial champions.

As a result, Europe has achieved a 20 percent world market share in Information and Communication Technology (ICT), an achievement that many pre-JESSI saw as hopeless. Within this, semiconductors have become one of the strongest European ICT segments, underpinning the achievements in all of the other sectors.

In order to further enhance European ICT competitiveness, a follow-on programme, CATRENE, was started in 2008 with the vision to achieve **"Technology Leadership for a competitive European ICT industry"**.

CATRENE is a four year programme, starting 1 January 2008, but extendable by another four years through 31 December 2015. In the period covered by this evaluation, CATRENE labelled 24 projects, of which 17 were looked at in detail, the other 7 having been cancelled after labelling for reasons outside of the control or influence of the CATRENE organisation. Most of these projects are still ongoing and the results anticipated cannot yet be measured. All projects of MEDEA+ Phase 2 were analysed as to their usefulness and purpose, although some are still ongoing.

Future Horizons believes Europe has every right to be justly proud of its collective achievements and we strongly believe that continued public support is the right approach for the next phase of CATRENE. Based on the results achieved to date, industry has clearly paid back the trust and commitment implied by receiving public investment and we have no hesitation in recommending a follow-on nanoelectronics support programme once the current CATRENE programme ends in 2011.

Summary Of Conclusions

- MEDEA+ Phase 2 and CATRENE's goals are in line with both Europe's strategic needs and the general development of the globalised nanoelectronics world. The achievements to date show an impressive range of results and the projects are in line with the ITRS roadmap or with state-of-the-art research activities;

Executive Summary

- Many of the MEDEA+ technology projects have been highly significant. For example the FOREMOST project commercialised the 45nm CMOS technology developed in the ESPRIT NANOCMOS project. 2T301: EAGLE and 2T304: LIQUID and other projects maintained European strength in advanced lithography (worldwide market-share >70 percent), whilst other projects covered topics such as advanced non-volatile memories, power devices, microwave devices and chip/package co-design. Looking at the whole list every project appears to have an obvious commercial advantage in their specialist area. Since many projects are completed quite recently, we expect more results to be made available soon. We believe that in all projects there is a fair balance between input in terms of person-years and results achieved;
- Europe now matching best in class in SOI and supplying >70 percent of the world's SOI wafers.
- Mature 3D integration technology platforms and innovative packaging SiP;
- MEDEA+ and CATRENE provide a platform for joint development, competences and standards, both horizontally and vertically within the supply chain. Examples are the demonstration of European solutions and standards for security and trusted computing. European smart card and security activities have created standards and technologies as enablers for new applications and secure services, dominating the global smart card market. In the trusted computing field, which is dominated by USA, the TSC project has created a European solution of key strategic importance;
- MEDEA+ is a real success story: essential breakthroughs have been achieved in a number of applications related to wireless broadband, multimedia systems (BluRay standard) and terminals (3DTV); essential contributions to automotive platform development, substantial achievements in reliability, safety and intelligent features for vehicles;
- MEDEA+ strongly advocates for more Electronic Design Activities in Europe. After releasing the first EDA roadmap in 2005, a new one was edited by CATRENE in 2009. It can be used as a yardstick for further activities. The roadmap is also well recognised by the ITRS organisation. Some EDA SMEs have achieved unique breakthroughs in e.g. simulation time reduction by intelligent data reduction;
- It is obvious, that the time span between time of labelling a project and real start date has to be significantly reduced, even more for bottom-up projects. The pace of change and technological development in the information economy is so furious that even a small delay in exploiting a commercial advantage, or technological invention, can mean millions of euro in lost sales and profits, and even the loss of the market itself.
- We believe CATRENE has adequate selection criteria in place during labelling, and appropriate project reporting and monitoring procedures in place to ensure the continuing high quality of the projects.

Executive Summary

- We are totally supportive of CATRENE as a concept and view the vast majority of current projects as valid, a good investment of public funds and capable of creating commercial opportunities for European companies.

Summary Of Recommendations:

- MEDEA+/ CATRENE played a decisive role for the value chain in nanoelectronics. Since nanoelectronic is a key enabling technology (KET) for Europe and the driving force for the development of future goods and services affecting almost all parts of our life, a strong position is key for European competitiveness. CATRENE has a unique position in relation to national and other supra-national R&D programmes due to its industry led bottom-up approach. The public authorities involved in CATRENE should therefore continue to support the second phase of CATRENE;
- We believe that if the companies released more information on the commercial success of products that incorporate projects funded under CATRENE then fewer doubts would be expressed on the effectiveness of the programme. We suggest this is made a condition for participation in CATRENE projects;
- There are several examples of SME success stories in the MEDEA+ programme. These should be published more clearly as a demonstration for other potential SME participants;
- CATRENE will have to master both 'More Moore' and 'More Than Moore' technologies. Without support for such advanced CMOS technologies, Europe will simply cease to be a player in advanced semiconductor wafer fabrication;
- The public authorities need to change the national approvals process to a parallel rather than serial process so that funds are released as soon as a project is approved by CATRENE.

Chapter 1 – Introduction

1 Introduction

Since the Ancient Greeks, pure scientific research has been financially supported by society or other patronage, with advancements from this research used to improve the lives of current or future generations. Later on, technology research was also supported, often for national security purposes, but again with a definite goal of improving society. Indeed, the origins of Silicon Valley can be traced back to the 1890s when Leland Stanford established Stanford University in Palo Alto with the express proviso that its students applied their learning for the benefit of mankind.

During the late 19th and early 20th century, manufacturing activities driven by science and technology research overtook food production, mining, housing construction and other activities as the major source of wealth creation in the industrialised nations. Since then these nations have become ever more dependent on the flow of scientific and technological advances to drive improvements in society.

Technology has driven the industrialisation of previously underdeveloped countries such as Korea, Taiwan, China, Malaysia and India as they sought to follow the post-war example of Japan in creating a modern wealthy society based upon the export of technology-based products. This, combined with the seemingly ever-increasing cost of technology research and the benefits of volume manufacturing, has created fragmentation of the market and specialisation in particular areas.

Whereas thirty years ago most industrialised nations could reasonably expect to play in most areas of technology selling predominantly to their home market, countries nowadays tend to specialise in fewer core areas targeted now at global markets, albeit whilst also seeking to maintain at least some presence in their non-core areas. Thus we see the situation now where Korea successfully exports televisions to almost all countries of the world; Germany, the US and Japan dominate world car production; the US and UK makes almost all of the world's jet engines, and so forth.

Even with this specialisation, the cost of researching and developing new technologies has risen dramatically over time. If left to normal market forces, these costs would cause the weaker companies involved to fail leaving only the stronger companies to dominate the world market. What has happened instead is that countries have decided to protect or encourage the growth of certain industries by a combination of strategic government purchasing, favourable tax regimes and outright subsidies.

This is not a new phenomenon of course but today some technology driven companies worldwide have become totally dependent on direct and indirect government support. Since this situation cannot easily be changed, it is up to governments to decide if a particular segment of technology is relevant to their national interests and if so, to put in the appropriate policies to properly support it.

This report reviews the current situation of supporting the development of nanoelectronics technology in Europe and comments upon its effectiveness and potential sustainability.

Chapter 2 – Micro/Nanoelectronics In Europe

2 Micro/Nanoelectronics In Europe

Whereas most modern technologies such as automotive products, pharmaceuticals, petrochemicals, computing and suchlike can be traced back to their initial creation within Europe, microelectronic and now nanoelectronic technologies have never been a core European speciality. The transistor was invented in the USA in 1947 and for many years this field was led by the USA and Japan, with production in Europe focused on serving local geographic needs.

The first integrated circuits were developed primarily for space and defence purposes, moving progressively into mainframe and mini-computers, neither of which were European core competencies, and by the mid-1970s into certain consumer products, primarily calculators and TVs. By this time almost all electronic products had been 'transistorised' but by and large the technology was not considered strategic.

The 1980s home computer revolution started to change this and the 'silicon chip' became a major focus of attention. Since then the number of products using ever more sophisticated ICs has grown hugely and almost every part of our lives are now dependent on these products. Even in the most traditional of industries, such as agriculture, livestock or bagged produce, products etc are electronically tagged and automatically tracked.

By the mid 1980s, European governments realised that Europe was lagging in the design and production of ICs and various support initiatives were created to address this situation. At the EU level, the experience of successfully co-ordinating nuclear research across Europe was extended to other fields under the ESPRIT Framework programmes and fundamental research into microelectronics gained support.

Another European research initiative, EUREKA, was officially launched in 1985 with a different strategy to ESPRIT in that it depended on the initiatives of participating organizations, i.e. it was a bottom up rather than the top down approach. The first major EUREKA project focused on developing high definition TV.

At the same time several governments, notably the UK and Ireland, encouraged Japanese and US companies to build semiconductor and end equipment plants in Europe using attractive subsidy packages to create production jobs. With relatively few exceptions, these activities mostly proved unsustainable, primarily because what Europe really needed was successful European companies capable of competing with the US and Japanese (Korea and Taiwan were not yet then a factor) world leaders.

Recognising this dilemma, driven by several charismatic European semiconductor and equipment company CEOs, a semiconductor-specific Joint European Submicron Silicon Initiative (JESSI) was launched in 1989 as a joint venture between ESPRIT and EUREKA. The purpose of JESSI was to develop advanced semiconductor technologies such the Europe could close the gap with its US and Japanese competitors. Although it took some time, JESSI and its MEDEA successor were a major success.

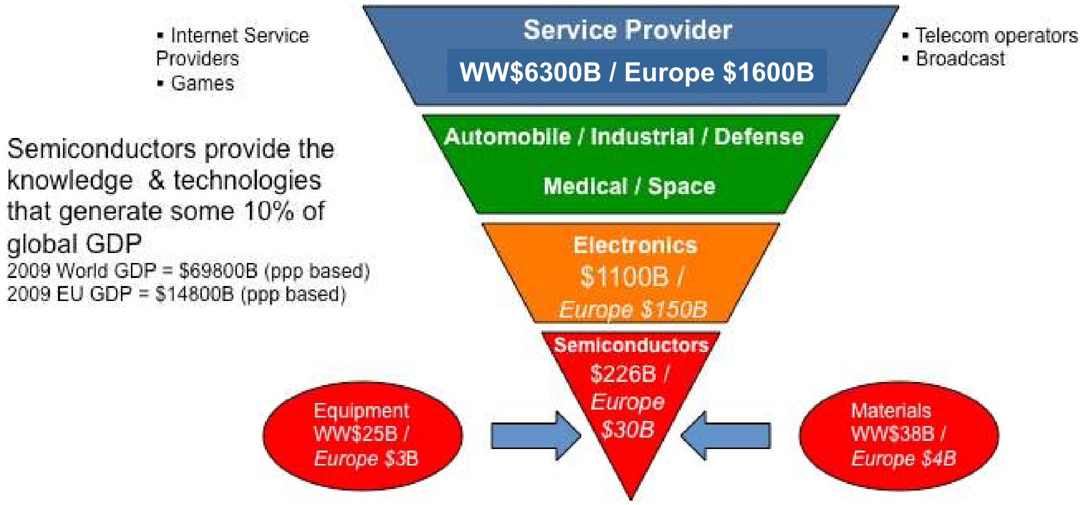
Chapter 3 – European Research

3 European Research

After the successes of these programmes, Europe had highly successful systems companies being supplied by an equally successful European semiconductor industry.

As can be seen from the diagram below, a relatively small value of semiconductors supports the larger electronics industry which in turn supports major industries such as automobile, industrial and defence as well as services such as telecommunications and entertainment. It is this importance that has led semiconductors to be recently recognised as a Key Enabling Technology (KET) by the European Commission.

Semiconductor - A Key Enabling Technology (2009 Data)



Source: EECA/ESIA

This structure is remarkably similar to another commodity that the whole world does recognise the value of and even goes to war over, namely oil. Oil underpins industries such as construction, transport, plastics, pharmaceuticals and even food production. Natural gas is following the same trends; especially worrying for Europe given it derives a large proportion of its needs from Russia, which routinely shuts off supplies, most notably to the Ukraine and thereby indirectly to Europe, for totally political purposes.

Because Europe is forced to obtain most of its oil and gas from outside of its borders and realises its wider sphere of importance, it goes to great lengths to protect these supplies. Our argument is that semiconductors, in particular wafer fabrication, is of equal importance and that if access to these supplies were ever to become restricted, whether for commercial or political reasons, then not only would Europe's electronics industry be at risk, the far larger industries supported by electronics would be negatively affected.

Chapter 4 – MEDEA+ & CATRENE Projects

4 MEDEA+ & CATRENE Projects

The current MEDEA+ and CATRENE projects are listed in the annex of the report produced by the CATRENE team. There are a wide variety of projects covering a wide range of topics. This chapter looks at each project in turn and provides an top-level assessment as to its usefulness and purpose.

MEDEA+

Many of the MEDEA+ technology projects have been highly significant. For example the FOREMOST project commercialised the 45nm CMOS technology developed in the ESPRIT NANOCMOS project. 2T301: EAGLE and 2T304: LIQUID and other projects maintained European strength in advanced lithography whilst other projects covered topics such as advanced non-volatile memories, power devices, microwave devices and chip/package co-design. Looking at the whole list every project appears to have an obvious commercial advantage in their specialist area. However, since so many are now completed, we would have expected more results to be made available.

The MEDEA+ application projects are also advantageous but we notice a lack of information justifying many of them. Of course these are projects where commercial sensitivity is the highest but we believe there should be more information on the target application provided.

The project that stands out head and shoulders above the rest is 2T204: ELIAS which covers the development of test methodologies for accelerated lifetime testing, especially for automobile applications. We recall being highly impressed with the presentation of the results of this project at the 2009 European Nanoelectronics Forum, as obviously were the judges for the Jean-Pierre Noblanc Award for Excellence that it duly won.

The MEDEA+ application projects have achieved a number of breakthroughs in the area of testing (2A702 NanoTEST), increase of design productivity (2A703, 2A704, 2A713, 2A714), reduction of power consumption (2A708), handling design complexity (2A717), rebustness and reliability in transport applications (2A701, 2A713), and enabled new business areas by working on multi-antenna and low cost radio systems (2A103, 2A105, 2A106).

In the multi-media area projects have been realised in order to enable European companies to stay in the market, dominated by the Asian companies. The project 2A201 BLAZE is a representative example for achieving time to market by being the first in the bluray application. It received the Jean-Pierre Noblanc Award in 2008. Project 2A302 Onom@Topic+ laid the basis for a strong European security solution enabling European identity card and governmental services.

In addition, Onom@Topic+ achieved several awards. With the project TSC, Europe becomes independent from other regions in the strategically important area of trusted computing.

Chapter 4 – MEDEA+ & CATRENE Projects

We also notice in the applications area a large number of what are effectively EDA projects, even though they were not always labelled as such. Europe is actually a hotbed for developing new ideas in EDA but is historically terrible at commercialising those ideas with at best developments end up in internal development methodologies complementing commercial toolsets but rarely is there any true commercialisation of these ideas. However in MEDEA+ we are assured that commercialisation of these projects does happen as for example the company Edxact.

In the MEDEA+ 2A704 ROBIN project, Edxact developed CAD tools for modelling interconnection networks. In the project simulation time reduction of 100x has been achieved with Model Order Reduction. Concepts are integrated onto partner's tools. Only in the third call of MEDEA+ second phase 3 projects out of 8 are effectively EDA projects including tool development.

CATRENE

Not surprisingly, CATRENE programme has a similar mix of projects that we will examine here in much more detail as most are currently in the early stages of their programmes.

Technology Projects

CT105: 3DIM3 does not give any details on what the actual 3D integration technologies being used are but this is definitely an important area for multimedia and mobile products so we would expect to see technologies such as stacked die and chip in board.

CT204: PASTEUR concerns RFID sensors. One would have expected the withdrawal of German support would delay the project significantly but it seems not. This does pose the question of just how important the tasks that have been withdrawn were and it may be the project listing process should have identified they were not critical. But in any case we believe this is a very worthwhile project which although not quite More than Moore is of course the type Europe can excel at using its existing fabs rather than needing access to new state of the art ones.

CT205: REFINED concerns embedded NVM at the 65nm node. Previous similar projects have been successful at 90nm and larger and so it makes sense to undertake this project. We are quite surprised and a little concerned to see that IMEC withdrew from this project as they are the source of much of the world's basic NVM technology.

CT206: UTTERMOST is the 32nm technology driver project. The cost of setting up these technologies in a fab is not a simple task and it will be necessary to have similar projects at 22nm and beyond. Without supported such projects Europe will simply cease to be a player in advanced semiconductor wafer fabrication.

CT207: COCOA is another 3D integration project but concerns the preparation of the die. This is a good example of a More than Moore technology that allows Europe to compete without the latest process technologies.

Chapter 4 – MEDEA+ & CATRENE Projects

CT301: EXEPT works on extreme UV lithography. Europe is of course the world leader in lithography solutions and it is essential we remain so. All the key companies and institutions are involved and although there is some slippage we are sure this, being one of the flagship CATRENE projects, it will be hugely successful.

CT302: TOETS tries to improve test methods by making it a fundamental part of the design flow. Improving test solutions could give our semiconductor companies, large and small, a commercial advantage over other competitors as a way of reducing the finished cost of IC dies. Test can represent up to half the cost of some ICs and so reducing this would be a significant move.

Application Projects

CA101: PANAMA does not say how the results expected from this project will be achieved but base station transceiver and handset power amplifier and antennae are critical to Europe so we presume this omission is for valid commercial reasons.

CA103: HERTZ concerns the intelligent home and control and optimisation of energy consumption. Again this fits in well with the European goals of efficiency.

CA104: COBRA appears to duplicate work already well established and shipping both in the US and the UK. The communications and media world does not need another parallel computing fabric. However it builds on existing IP for the intended applications. The project is also changing its membership and schedules making it very unstable but we are assured this does not weaken the project.

CA201: TS-CIMoHNET builds upon a number of projects such as TSC, BioP@ss, Open TC and Retrust both from the IST-FP6 programme. We were surprised that the world leaders in these technologies, ARM and Infineon, are not involved, but we are informed Germany will not fund security projects within Eureka so this is not the fault of CATRENE.

CA202: eGO covers a very important area of control using positional MEMS and sensors. These are both currently European strengths and this application should be in an excellent position to continue this success.

CA301: HiDRaLoN fits well with European plans to be strong in healthcare products both for worldwide success and to reduce the cost of healthcare within Europe. The goals appear focused and very worthwhile.

CA303: OPTIMISE surprised us in that German experts in such technology, for example Bosch, are not involved. However the goals are well defined and sensible and the delay in beginning the project was unfortunate but not fatal.

CA402: THOR appears to keep Europe as a leader in another area, namely that of power devices and is essential to many industries.

CA501: COMCAS focuses on the design flow for extreme low power solutions with high complexity (heterogeneous multi-chore architectures) finding a trade-off between performance and power consumption in the area of communication applications. It seems rather odd in that it does not appear to involve ARM, the

Chapter 4 – MEDEA+ & CATRENE Projects

processor design company, given the processor is such a key part of the system. We realise the UK will not fund CATRENE projects but we are sure the project would be more efficient if ARM were directly involved, even if the other partners had to pay them to do so.

More importantly we believe STNoC is a synchronous network-on-chip (NoC) and that several partners who were previously working on asynchronous networks on the MEDEA+ LoMoSa+ and other projects agree this was an incorrect choice. It is generally accepted in the industry that asynchronous NoCs are the correct way forward as has been demonstrated by the world leading French firm Arteris and others. We understand STNoC was chosen to build upon existing multi-media IP but this has to be seen as a stop-gap and future projects should concentrate on the more advanced asynchronous NoCs again.

CA502: SEEL is one of several lighting research projects, others we know of being financed by the EU and the UK government. We assume this will feed from the EU research that has many of the same members.

Summary

We are totally supportive of CATRENE as a concept and view the vast majority of current projects as valid, a good investment of public funds and capable of creating commercial opportunities for European companies.

There are two projects (COBRA and COMCAS) that we personally would not have approved in their current form, as we believe a major part of one is reinventing the wheel and the other is technically flawed. That said, we have only limited knowledge of their workings and are not sure how projects proposed in the call for projects are selected for listing but it may be there needs to be greater technical critiquing at this point.

It is also noticeable that in CATRENE there appear to be no straightforward EDA tools in development, a major change from MEDEA+, and that development has moved onto methodologies. We are not sure if this was planned, a result of ENIAC now covering EDA projects or just a lack of proposals. It is an area however we fell should not be neglected in future calls.

Chapter 5 – Publication Of CATRENE Projects

5 Publication Of CATRENE Projects

CATRENE projects input directly into planned commercial programmes and so obviously any information that is published has to be carefully considered as to whether its release would be commercially damaging.

That said, CATRENE projects do enjoy public funding and these commercial aspects need to be balanced against the need for funding transparency. Publishing results also serves a useful purpose in highlighting the effectiveness of the programme.

Whereas some projects do publish such information, this is not consistently applied across the full gambit of projects others are less forthcoming and we recommend a more formal guidance on this be introduced by CATRENE.

Chapter 6 – Interactions With ENIAC

6 Interactions With ENIAC

ENIAC is an EU-sponsored programme running in parallel with CATRENE. On occasions this concurrency has been a potential source for confusion and overlap concern. We believe these concerns are unfounded and that the two programmes compliment each other.

One of the biggest differences between the two programmes is that ENIAC generally performs pre-competitive research whereas CATRENE projects are closer to market. This factor alone is sufficient to justify two concurrent programmes.

We are happy to report CATRENE has established a healthy working relationship with ENIAC, witnessed by the fact two parties are co-hosting the annual European Nanoelectronics Forum in Madrid later this month.

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