Programme Review
Excerpts Year 2012

EUREKA Σ! 4140

Programme Review Excerpts Year 2012

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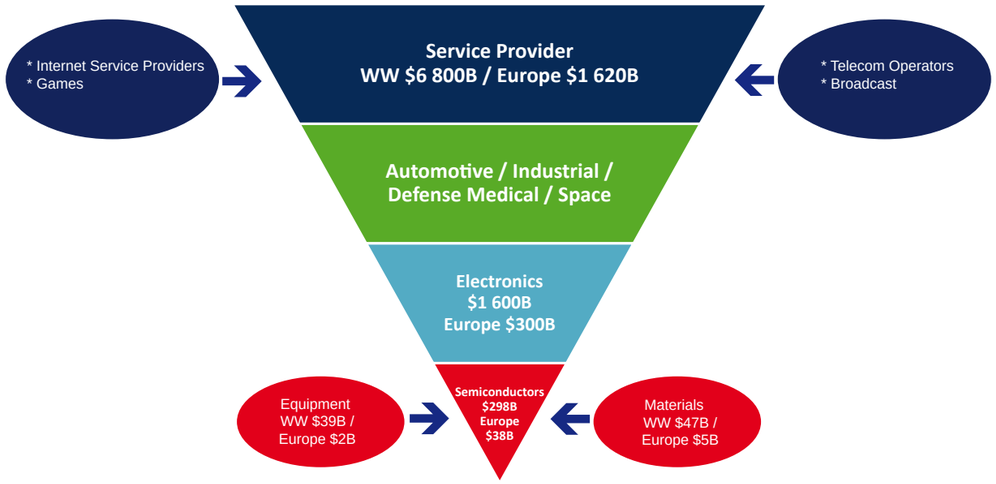
INTRODUCTION

INTRODUCTION

The impact of the semiconductor industry is undeniable today for the European economy and the same holds true for the rest of the world. Nanoelectronics are touching every aspect of our lives and are omnipresent. The technology is present in your credit card, at the airport when you go through security, in your cell phone, on your desk, in your car, in your home, in the train, on a plane… everywhere.

The semiconductor industry enables nearly 10% of global gross domestic product (GDP) and since nanoelectronics are crucial for electronics and IC technology, the semiconductor market is increasing at double the rate of GDP growth. In Europe, alone, the sector is worth almost 40 billion dollars. A report issued by the European Union in 2011 stated that over the past decade, micro- and nanoelectronics as well as their natural downstream sectors created more than 700 000 jobs in Europe.

The pyramid of wealth



Semiconductors provide the knowledge & technologies that generate some 10% of global GDP

2010 World GDP = $73300B
2010 EU GDP = $15040B (ppp based)
ppp = purchase power parity

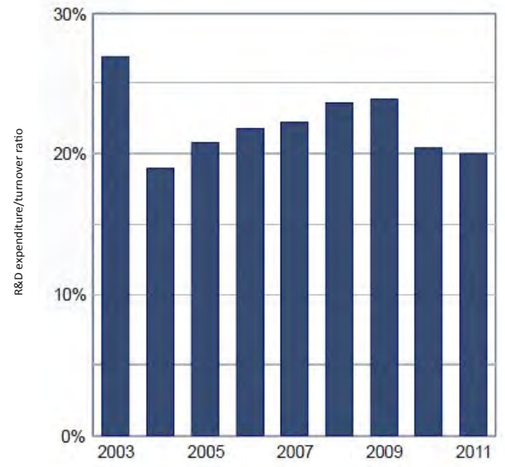
Source: DECISION, ESIA, Future Horizons, IMF, WSTS

Nanoelectronics have and will continue to facilitate new, innovative and practical solutions for today's societal challenges. In the foreseeable future, the role of electronics and information systems will grow as European society faces structural problems such as an ageing population, exploding healthcare costs, transportation bottlenecks, rising energy costs and the need to increase productivity to remain competitive on a worldwide basis. European citizens expect better health systems, safer cars, optimized energy management, enlarged telecommunications and information access, better entertainment and security everywhere.

In 2009, the importance of the semiconductor industry for Europe was made official. The European Commission identified nanoelectronics as one of the six Key Enabling Technologies (KET) – recognized as playing an increasingly vital role in developing the required industrial and technological base indispensable for a competitive European economy and growth.

For Information and Communication Technology, the innovation race is not over. There is still a need to go further with miniaturization, to integrate technology into new applications and to increase functionalities. Since this race is continuing, Europe must also continue in order to remain competitive. The future will depend on Europe's capacity to remain state of the art and to innovate. This goal, however, has a cost. The ratio between R&D expenditure and turnover for nanoelectronics in Europe is the highest of all industries, exceeding 20%. To keep this level of investment in R&D, a strong commitment from both the European nanoelectronics community and the public authorities is necessary.

European R&D expenditure/Turnover ratio in the semiconductor field*



Source EECA ESIA

For more than two decades, the EUREKA JESSI, MEDEA, MEDEA+ and CATRENE programmes have been working with Europe's R&D community and public authorities to promote European leadership in the field of nanoelectronics. They have helped Europe's industry reinforce its position in semiconductor process technology, manufacturing and applications, and to become a key supplier to markets such as, but not limited to, telecommunication, automotive and transport, industrial applications, equipment and materials while addressing emerging societal needs. The strategic guidelines for the current CATRENE programme take into account Europe's societal challenges and aim to identify the potential market opportunities resulting from them.

CATRENE launched its 5th call in 2012 and is the largest EUREKA Cluster in terms of investment. It has well over 300 partners from 20 different countries. Public support from these European Member States, in terms of funding but also of a levelled playing field, for programmes like CATRENE is crucial in order for the region's industry to face the growing and sometimes overwhelming competition from developed and emerging economies such as East Asia.

As agreed in November 2010 when the CATRENE programme received the green light for prolongation, a mid-term assessment of the tool by the participating Public Authorities was launched in October 2012. The CATRENE Office, as well as many of the partners involved in CATRENE programme, have contributed to the evaluation process through information sharing and interviews. A final decision on the continuation of CATRENE until 2015 and beyond is expected by November 2013.

Chapter 1

CATRENE PROGRAMME OVERVIEW & SEMICONDUCTOR MARKET

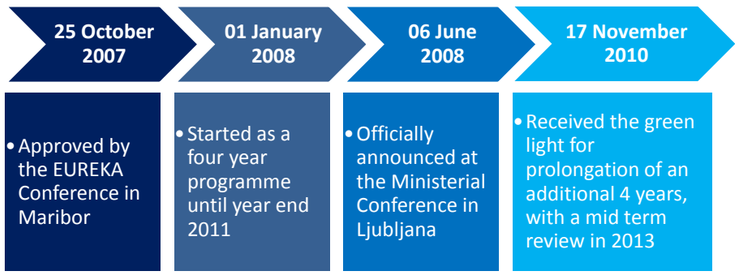
A. CATRENE PROGRAMME OVERVIEW: A PUBLIC PRIVATE PARTNERSHIPS FOR EUROPEAN CO-OPERATIVE R&D IN MICRO- AND NANOELECTRONICS

1. Introduction

It is the ambition of Europe and of European companies to deliver micro- and nanoelectronic solutions that respond to the society at large while improving the economic prosperity and reinforcing the ability of its industry to be at the forefront of the global competition.

The CATRENE cluster programme (Σ! 4140) builds on the successes of its predecessors JESSI, MEDEA and MEDEA+ with the aim of fostering the continued development of a dynamic European ecosystem with the critical mass necessary to compete at a global level.

Fig. 1.0: Milestones for CATRENE



Since its official launch at the beginning of 2008, the CATRENE programme brings together **all key actors of the semiconductor value chain** – including applications, technology, materials and equipment suppliers as well as large companies, small and medium-sized enterprises, research organisations, academia - around market opportunities while addressing societal challenges. It has also been able to maintain the strong points of its predecessors in terms of efficiency, flexibility and involvement of public authorities.

A mid-term evaluation of CATRENE was launched in October 2012. The CATRENE Office, as well as many of the partners participating in the Programme, have contributed to the process through information sharing and testimonials. The outcome of this evaluation, which will be known by November 2013, will provide the basis for the orientation of CATRENE until 2015 and beyond.

Micro- and Nanoelectronics: A Key Enabling Technology for EUROPE

In 2009, the European Union identified Key Enabling Technologies (KETs) for their potential impact in strengthening Europe's industrial and innovation capacity. In particular, KETs were recognized as playing an increasingly vital role in developing the required industrial and technological base indispensable for a competitive European economy and growth.

The following six KETs were defined: nanotechnology, micro- and nanoelectronics including semiconductors, advanced materials, photonics, industrial biotechnology and advanced manufacturing systems.

A High Level Expert Group on KETs was created and tasked with the elaboration of a coherent European strategy. Recommendations for the advancement of KETs in Europe were given in June 2011, spanning the entire value chain from the generation of ideas to their commercialisation and covering the areas of technological research, product development and globally competitive manufacturing.

For nearly 20 years now, CATRENE and its predecessor programmes have been actively contributing to the deployment and mastering of the KET, micro- and nanoelectronics in Europe.

2. A successful EUREKA cluster

EUREKA Clusters are a EUREKA success story. In terms of project funding, they represent more than 70% of the EUREKA portfolio. They feature a high industrial participation, with an extensive – and increasing – level of SME participation. The success of the Clusters relies on the opportunity for member countries to support national companies in major strategic technology fields which are in line with domestic priorities. The willingness of member countries to provide funds is connected to the expectations in terms of economic impact, or contribution to resolving the "Grand Challenges" for their country in the short and medium-terms.

CATRENE is the largest EUREKA Cluster in terms of investment. For more than two decades, the EUREKA JESSI, MEDEA, MEDEA+ and CATRENE programmes have made it possible for Europe's industry to reinforce its position in semiconductor process technology, manufacturing and applications, and to become a key supplier to markets such as, but not limited to, telecommunication, automotive and transport, industrial applications, equipment and materials while addressing the emerging societal needs.

In 2010, CATRENE and other EUREKA Clusters decided to create an Inter-Cluster Committee with the aim of improving communication and cooperation within the EUREKA network. The first spokesperson of the Intercluster Committee was the CATRENE Chairman; followed by the Chairman of Itea2 and then by the Chairman of Celtic Plus. The prevailing Committee spokesperson is invited to the EUREKA decision body meetings in order to reinforce the interaction between the EUREKA network, Public Authority representatives and the Clusters. Regular inter-cluster meetings are being held and operational synergies are increasing.

The EUREKA clusters work together in order to best meet the requirements of their project participants over time. Such efforts, for example, have led to intercluster cooperation on project level. The merge of multiple technologies within a nanoelectronic solution that requires enlarging system knowhow in nanoelectronic design houses as well as the increasing complexity of system solutions are the main factors pushing towards further cooperation. The co-labelled project THOR is an example of a successful cooperation between CATRENE and EURIPIDES.

3. CATRENE: Strategy and work programme

CATRENE follows the strategic guidelines outlined in the **Vision, Mission and Strategy (VMS) document** inclusive of the **CATRENE White Book**.

3.1 Strategic documents

The **Vision, Mission and Strategy (VMS)** has been elaborated in 2010 by major industrial and research organisations as a common document providing a working framework for both European funding tools focused on nanoelectronics: CATRENE and the ENIAC JU. The VMS paper is in full accordance with recommendations given by Public Authorities but provides more details in many aspects, priorities, focus and implementation aspects in line with the proposed R&D and industrial policy.

Fig. 1.1: Outline of VMS document

Vision

The European micro- and nanoelectronics industry value chain will guarantee the controlled access to information and communications technology (ICT), applications and products for a smart, sustainable and inclusive European 2020 society.

Mission

The mission of the European micro- and nanoelectronics industry value chain is to progress and remain at the forefront of state-of-the-art innovation in the further miniaturisation and integration of devices, while dramatically increasing their functionalities.

Strategy

- The first pillar of the strategy for the European micro- and nanoelectronics industry is therefore to build on its leading position in specific technology and application domains.
- The second pillar of this strategy is for Europe to be positioned at the forefront of new emerging markets with high potential growth rates and to become a world leader in these domains.
- The synergy of these two pillars will enable the European semiconductor industry to expand its position in More-Moore as well as its leading position in More-than-Moore technologies, providing optimised systems solutions adapted to the demand of European original equipment manufacturer (OEM) leaders in the new emerging markets.

The latest **CATRENE White Book** is a combination of the VMS parts A, B, C and annex 1. It describes, in detail, the work programme of CATRENE in both Applications and Technology.

3.2 Work programme

CATRENE is bottom up organised. It focuses more on an evolutionary approach, stand-alone systems, improvement of existing systems and solutions, specific appliances, tool and technology development, equipment and material development, like (non-exhaustive):

- Devices and products for automotive, transport, industry, automation and energy efficiency;
- Devices for health care and medical application;
- Devices for communication systems (One chip phone, high speed optical transceivers…);
- Sensors and actuators, MEMS;
- Design Technology (Architectures, Design Methods and Tools, EDA, TCAD, DfM, DfR, DfT …);
- More Moore and More than Moore technology development;
- Specific equipment and material development (lithography tools, SOI, SiC, etc);
- 3D technologies and associated CAD tools;
- 450 mm equipment and materials;
- Manufacturing sciences.

3.2.1 Technology domain

The technology programme will support the following work areas as defined in the VMS:

1. Semiconductor process and integration;
2. Equipment, Materials and Manufacturing.

3.2.1.1 Semiconductor process and integration

For the coming years, CMOS will remain the basic technology for integrated circuit, even if research on alternative devices has led to promising results. The International Technology Roadmap for Semiconductors (ITRS) provides global long trends, which drive the continuous evolution and will pave the way for the technological breakthroughs. These alternative devices coming from the diversity will bring new ideas/options to the CMOS process and will contribute to the integration of new materials, equipment/techniques and will provide new sources of technological breakthroughs.

The related technologies are:

- More Moore Technologies: Technologies platform for the next generation core CMOS processes and advanced nodes development.
- More than Moore technologies: Technologies platform for CMOS process options and Non-CMOS technologies, e.g. for RF, Sensors and actuators, power technologies.
- Heterogeneous integration technologies: Silicon in Package, System on Chip, Bio technologies integration, photonic devices...

3.2.1.2 Equipment, materials and manufacturing

This work area is an indispensable enabler in the supply chain of future semiconductor applications. The rapid evolution of the semiconductor industry is supported by the timely development of equipment, materials and processes.

This work area leads (list not exhaustive):

- the innovations for the advanced node for 22 nm and below,
- the innovations for more than Moore options and heterogeneous integration,
- the manufacturing science and the cross cutting technologies,
- the 450 mm supply chain: tools and materials.

3.2.2 Applications domain

Applications in CATRENE projects being either:

1. An application which uses a new technology in order to demonstrate the performance of a new process with the possibility of sub-systems, or building blocks being developed to compare performances with existing state of the art. For example, the new MEMS technology which offers a denser solution for RF.
2. Or, the definition and development of new sub-systems/building blocks for a given/existing

application, for example a new processing module or an innovative wireless modem solution for 3.5G mobiles.

3. Or, a new platform or solution for an existing application or system: e.g. innovative device/ product.

A key element common to these projects is Intellectual Property protection.

The Applications programme will support the application work areas as defined in the VMS for:

1. Communication and digital lifestyle,
2. Safety and security,
3. Automotive and transport,
4. Health and ageing society,
5. Energy efficiency and,
6. Design technology.

3.2.2.1 Communication and digital lifestyle

This work area encompasses devices, improvement of existing solutions and stand-alone complex products (e.g. LTE solutions, parallel antennas use, MIMO, RF technologies for sensor network, high speed optical communication systems,…). This list of examples is not exhaustive.

3.2.2.2 Safety and security

The emphasis is placed, both, on the improvement of existing solutions and stand-alone complex products (e.g. trusted platforms, smart-card security issues) as well as the definition of novel solutions in order to strengthen the leading position of Europe in this domain. This list of examples is not exhaustive.

3.2.2.3 Automotive and transport

This work area deals with devices and stand-alone complex products for automotive, transport and industrial applications. Special attention is given to introduction of multi-core technology, advanced reliability research (e.g. EMC), reliability and safety from components (e.g. sensors) subsystems, reliability, safety in operation, control, communication, appropriate multi-access/multi standard communication gateways, and intelligent electronics for security and privacy protection. This list of examples is not exhaustive.

3.2.2.4 Health and the ageing society

The focus lies on devices for healthcare and medical appliances. Examples are e-inhalers, MEMS actuators coupled with low power logic and energy scavenging, improved and combined image detectors for more precise and earlier detection, bio-sensors. This list of examples is not exhaustive.

3.2.2.5 Energy efficiency

In this area CATRENE focuses on new materials, devices and stand-alone complex products. Especially power efficient designs in devices have the priority in the context of reduction of energy consumption of electronic components. This list of examples is not exhaustive.

3.2.2.6 Design technology

One of the main focuses of the application programme is Design Technology. Design Technology is split into application driven (EDA, Electronic Design Automation) and physical and manufacturing driven Design Methodologies and Tools (TCAD, Technology Computer Aided Design).

The programme is led by the (internationally recognised) European Design Automation Roadmap. CATRENE will continue to play an important role in maintaining the roadmap. CATRENE organises a Design Technology conference every year since 1998 in order to disseminate the programme results.

3.3 Conversion table (Work areas CATRENE Calls 1, 2, 3 to CATRENE Calls 4, 5, 6)

The work areas, as described above, are applicable to Calls 4, 5 and 6 of the CATRENE programme. They have been redefined to correlate with the “Vision, Mission and Strategy” document published in 2011.

The following table details the conversion of work areas from CATRENE Calls 1, 2 and 3 to CATRENE Calls 4, 5 and 6:

Table 1.2 Conversion table: CATRENE work areas

CATRENE Call 1, 2, 3	CATRENE Call 4, 5, 6…
▪ *CA 1 = High quality, high speed user-centred communications systems*	▪ **Communication and digital lifestyles = CA 1**
▪ *CA 2 = Smart card system, trusted platforms and secure application*	▪ **Safety and security = CA 2**
▪ *CA 3 = Electronics in transportation for safety and security, environmental protection and communications*	▪ **Automotive and transport = CA 3**
▪ *CA 4 = Healthcare devices and system*	▪ **Health and the ageing society = CA 4**
▪ *CA 5 = Energy-efficient devices and Energy control systems*	▪ **Energy efficiency = CA 5**
▪ *CA 6 = Devices and systems for digital entertainment*	▪ **Communication and digital lifestyles = CA 1**

CATRENE Call 1, 2, 3	CATRENE Call 4, 5, 6…
▪ *CT 1 = Electronic design automation for advanced SoC and SiP design*	▪ **Design technologies = CA 7**
▪ *CT 2 = Process development (More Moore & More than Moore and heterogeneous system integration)*	▪ **Semiconductor process and integration = CT 2**
▪ *CT 3 = Manufacturing science (cross cutting technologies, equipment & materials)*	▪ **Equipment, materials and manufacturing = CT 3**
▪ *CT 4 = Smart sensor and actuator systems*	▪ **Smart sensors / actuators are split between above listed applications, Semiconductor process and integration as well as, Equipment, materials and manufacturing (heterogeneous system)**

4. CATRENE Programme: facts and figures

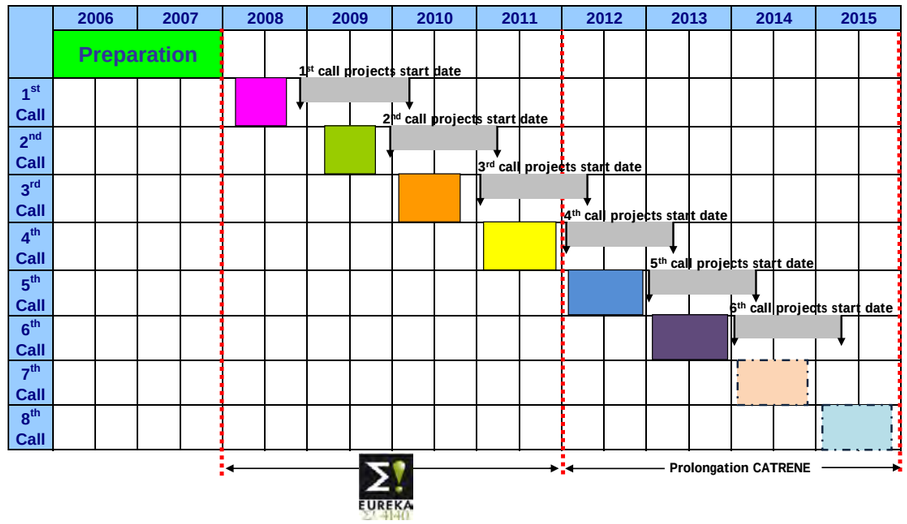
4.1 Overall timing of the CATRENE programme

A call for submission of project proposals is launched every year. In addition to the calls launched, unsolicited project proposals can be submitted at any time during the year.

Each year in preparation of the calls, a brokerage event is commonly organized by CATRENE and AENEAS (the industrial association representing R&D actors in the ENIAC Joint Undertaking). The aim of the event is to bring together the main actors of the European nanoelectronics R&D community and to facilitate exchanges in order to generate ideas for proposals and to start consortia preparation.

A mid-term assessment of CATRENE is on-going in 2013 to decide on the implementation of the last phase of the current programme (Call 7 and 8) as well as its operation beyond 2015.

Table 1.3: CATRENE overall agenda and timing



4.2 Status of CATRENE calls

The CATRENE programme opened its 1st Call for Project Proposals on 29 February 2008. Today, a total of 5 calls have been launched resulting in 37 labelled projects. As of 2S 2012, 9 CATRENE projects have successfully ended.

Contrary to the predecessor programme MEDEA+, there are in CATRENE quite a number of project cancellations: national eligibility criteria, funding constraints and in some countries even a reduced funding volume. These issues are creating many project change requests and cancellation of labelled projects.

Further details on each call are provided in Table 1.4.

Table 1.4: CATRENE calls and projects (status of as 2S-2012)

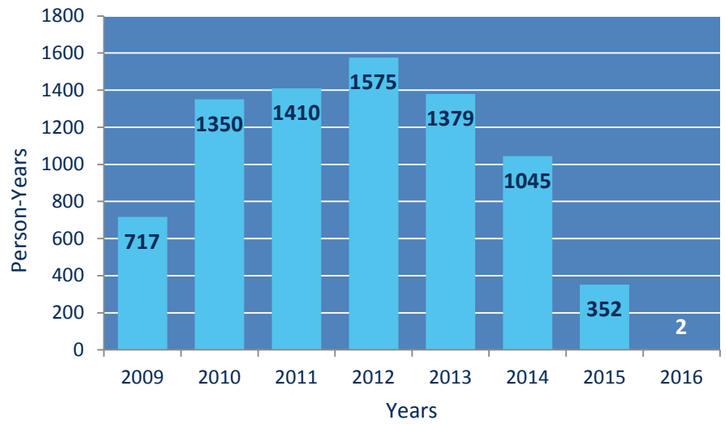
				Out of the labelled are:			
Call	PO received	FP received	Labelled	Cancelled /merged/ transferred/ suspended	Successfully Ended	Active	Out of active are in start-up phase
1st Call	**17**	**14**	**14**	**5**	**8**	**1**	**0**
Applications	10	8	8	3	4	1	0
Technologies	7	6	6	2	4	0	0
2nd Call	**14**	**10**	**10**	**3**	**1**	**6**	**0**
Applications	9	7	7	3		4	0
Technologies	5	3	3	0	1	2	0
3rd Call	**15**	**10**	**10**	**3**		**7**	**0**
Applications	7	4	4	2		2	0
Technologies	8	6	6	1		5	0
4th Call	**19**	**14**	**10**	**1**		**9**	**2**
Applications	10	8	7	1		6	1
Technologies	9	6	3	0		3	1
5th Call	**8**	**5**	**5**	**0**		**5**	**3**
Applications	**5**	**3**	**3**	**0**		**3**	**1**
Technologies	**3**	**2**	**2**	**0**		**2**	**2**
Per 2S 2012	**73**	**53**	**49**	**12**	**9**	**28**	**5**

With the prolongation of the CATRENE programme, further calls for submission of project proposals are planned in the years to come.

4.3 Overview of CATRENE projects (resources, participants, work areas)

The following figures provide an overview of CATRENE project resources (in PYs), of their participants and of their related work area.

Fig. 1.5: CATRENE 1st, 2nd, 3rd, 4th, & 5th* call labelled resources Total PYs: 7,823*



* This figure does not include the person years of MEDEA+ projects which continued running until 2010. Figure based on statistics from 2S 2012.

Fig. 1.6: CATRENE resources per country as per 2S-2012

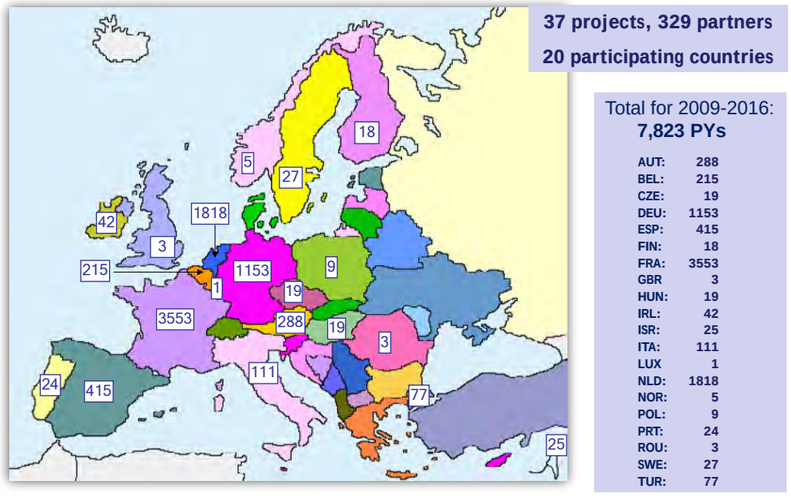


Fig. 1.7: CATRENE labelled projects – split by work area

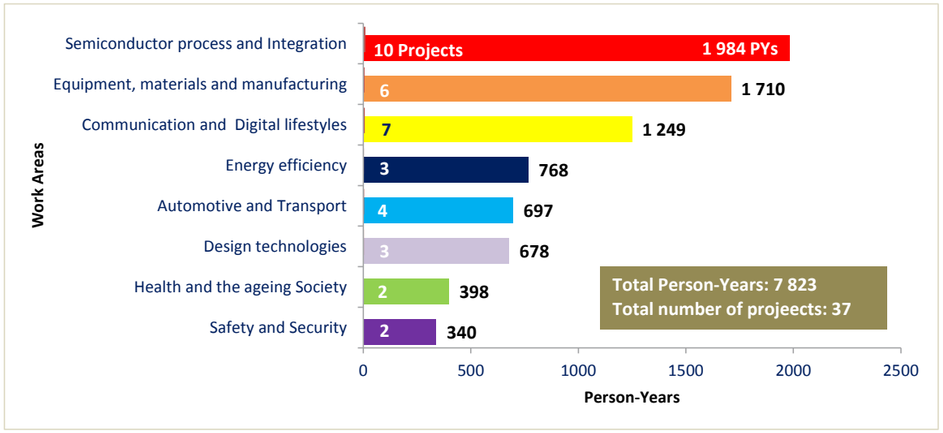
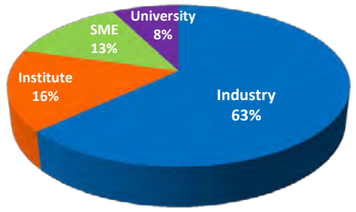
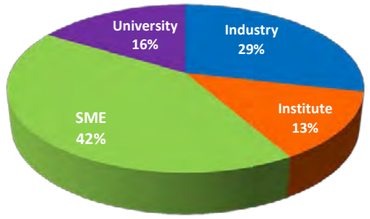


Fig. 1.8: Structure of CATRENE projects

Total Resources: 7,823 PYs



329 participants from 20 countries



In the CATRENE White Book (VMS and Annex 1), a matrix of application work-areas based on societal needs and grand challenges has been defined. These needs and challenges are expected to have growing market impact, not only in Europe but worldwide: high quality employment and value creation will materialize, and these elements are strategic for Europe and European companies.

The focus matrix below shows the areas in which CATRENE projects are contributing to solutions for these challenges. As can be seen below, most of the projects are addressing several societal needs and challenges.

Table 1.9: CATRENE focus matrix

PROJECT NAME	Communication & Digital Lifestyle	Safety & Security	Automotive & Transport	Health and the Ageing Society	Energy Efficiency	Design Technologies	Semiconductor Process & Integration	Equipment, Materials & Manufacturing
CA101 PANAMA	**				*			
CA103 HERTZ	**				*			
CA104 COBRA	***					*		
CA109 SHARP	*			*		***		
CA110 APPSGATE	**			*	*			
CA111 UltraHD-4U	***							
CA112 HARP	**		*		*	*		
CA202 eGo	*	***						
CA206 NewP@ss		***						
CA301 HiDRaLoN	*		*	*				
CA303 OPTIMISE			**		*	**		
CA308 ICAF	***	**						
CA310 EM4EM			***			**		
CA402 THOR			*	*	*	*		
CA403 RELY			*	*		***		
CA501 COMCAS	**				**	*		
CA502 SEEL			**		***			
CA505 BENEFIC	*				**	**		
CA701 H-INCEPTION						***		
CA703 OpenES	*		*			***		
CT105 3DIM3	*					**	*	

PROJECT NAME	Communication & Digital Lifestyle	Safety & Security	Automotive & Transport	Health and the Ageing Society	Energy Efficiency	Design Technologies	Semiconductor Process & Integration	Equipment, Materials & Manufacturing
CT204 PASTEUR				*			***	
CT205 REFINED						*	***	
CT206 UTTERMOST						*	***	
CT207 COCOA						*	**	*
CT208 REACHING 22						**	**	
CT209 RF2T4Z SISOC	*					*	***	
CT210 DYNAMIC-ULP	*					**	*	
CT213 3DFF				*	*	*	**	
CT214 EuroProFILS				**			**	
CT301 EXEPT								***
CT302 TOETS								***
CT305 SOI 450								***
CT306 NGC 450								***
CT312 MASTER_3D								***
CT315 EmPower			*		**		*	
CT402 9D-Sense		*		*		*	**	

B. SEMICONDUCTOR MARKET

1. General market overview

The global semiconductor market achieved the largest dollar increase in its history in 2010, courtesy of a boom in DRAM and NAND sales that benefitted memory suppliers. Worldwide semiconductor revenue amounted to US$298.3 billion in 2010, up from US$226.3 billion in 2009. The increase represented a progress of almost 32% for the year.

For 2011, a difficult year for the world-wide economy, an increase of 0.4% worldwide was reported with considerable divergence between the regions.

The Autumn 2012 forecast by WSTS revised statistics downwards for both 2012 and 2013 with regards to their Spring 2012 forecast due to the "growing uncertainty of the world economy including China's slowdown". Accordingly, the world semiconductor market in 2012 was estimated at US$290 billion bringing it down by 3.2% with regards to 2011. The last WSTS forecast proved to be accurate and in fact, actual 2012 data at the world level was valued at US$291.5 billion (with a decline of 2.7% with regards to 2011).

For 2013, WSTS does not foresee a further reduction of the world semiconductor market but rather a growth of 4.5% equalling a total of US$303 billion. So far, no revision has been released for the 2013 forecast which will be available in May.

Similar growth (5.2% or US$319 billion) is anticipated in 2014 by WSTS.

Table 1.10: Semiconductor market forecast by regions

REGION	2011		2012		2013		2014		2015	
	US $B	2011 vs. 2010	US $B	2012 vs. 2011	US $B	2013 vs. 2012	US $B	2014 vs. 2013	US $B	2015 vs. 2014
AMERICAS	55.2	2.8%	52.8	-4.4%	54.7	3.7%	57.3	4.8%	59.6	3.9%
EUROPE	37.4	-1.7%	33.4	-10.7%	33.7	0.9%	35.2	4.5%	36.4	3.5%
JAPAN	42.9	-7.9%	42.0	-2.1%	43.4	3.3%	45.4	4.4%	46.2	1.9%
ASIA/ PACIFIC	164.0	2.5%	161.7	-1.4%	171.2	5.9%	180.9	5.6%	188.8	4.4%
WORLD	299.5	0.4%	290.0	-3.2%	303.1	4.5%	318.8	5.2%	331.1	3.9%

Source: WSTS Forecast Fall 2012

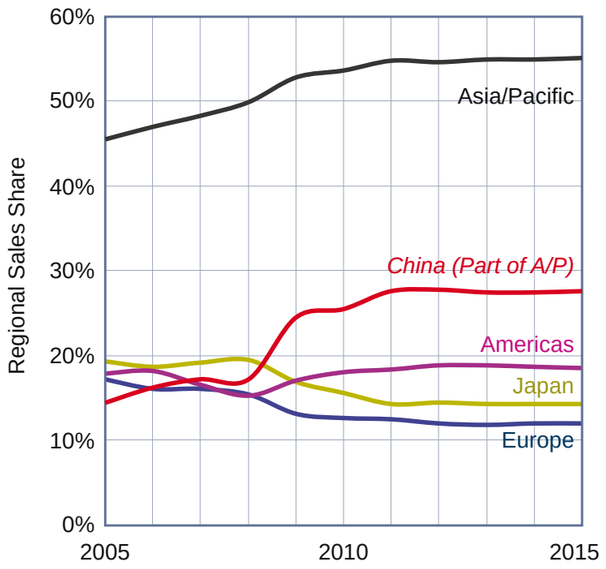
WSTS predicted a decline for all geographical regions in 2012; however, the European market is the hardest hit with -10.7% (US$33 billion for 2012) with regards to 2011.

Table 1.11: Forecast of regional sales share

REGION	2011	2012	2013	2014	2015
Americas	18.4%	18.2%	18.1%	18.0%	18.0%
Europe	12.5%	11.5%	11.1%	11.0%	11.0%
Japan	14.3%	14.5%	14.3%	14.2%	14.0%
Asia Pacific	54.8%	55.8%	56.5%	56.8%	57.0%

Source: WSTS Forecast Fall 2012

Fig. 1.11 (b): Share of regional sales and forecast

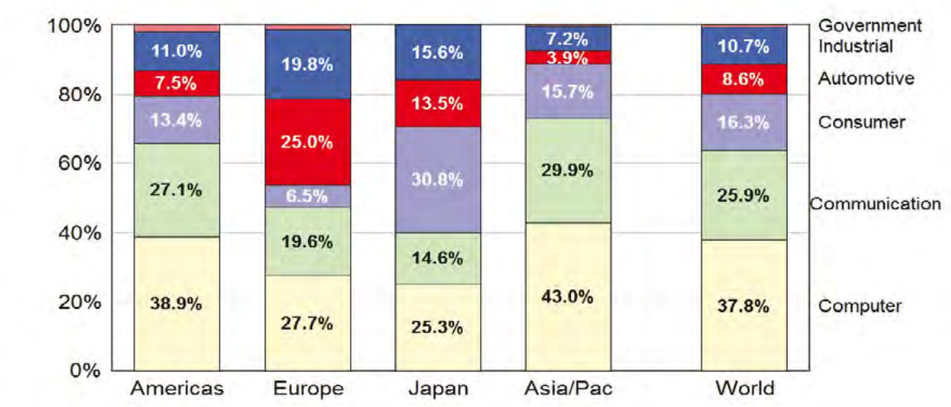


Source WSTS and EECA ESIA

2. Strengths and demand by region

The figure below (fig. 1.12) shows the particular strengths of each region by Application. The main products for the Americas and Asia market are computer and communication while Japan holds a lead on High end consumer products. The demand by application in Europe is well distributed, with particular demand in automotive and industrial electronics.

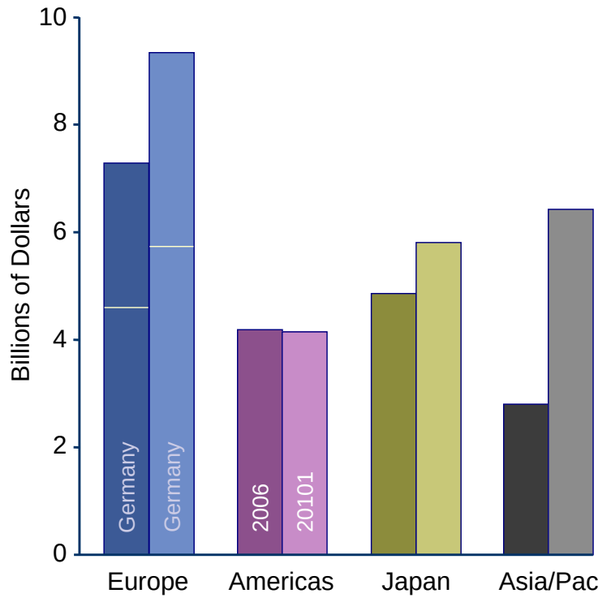
Fig. 1.12: Regional demand by application (2011)



Source EECA ESIA

Europe dominates the market of the automotive semiconductors with a 36% share. The main reasons for this European success include proximity to customers, highly qualified development engineers and ASICs in More-than-Moore technologies.

Fig. 1.13: Market by region of automotive semiconductors (2006/2011)

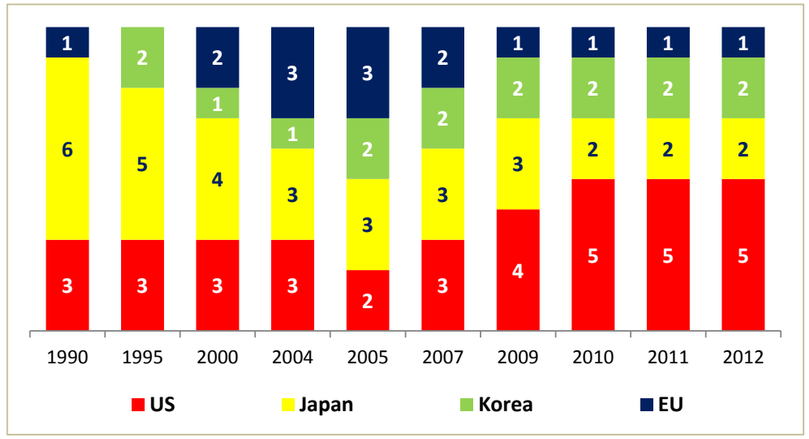


Source WSTS, ZVEI, EECA ESIA

3. Ranking and revenue

One European company, STMicroelectronics, remains in the top ten semiconductor companies. The American company, Intel dominates the top ten ranking and according to IHS iSuppli, in 2011 it attained its highest annual market share in more than 10 years. Intel's strong position was further boosted by the acquisition of Infineon's wireless business unit. IHS iSuppli lists further elements that have had an effect on the long term ranking indicated in Figures 1.14 and 1.15 including the acquisition of National Semiconductor by Texas Instruments, the acquisition of Atheros Communications by Qualcomm and the sale of Sound Solutions by NXP.

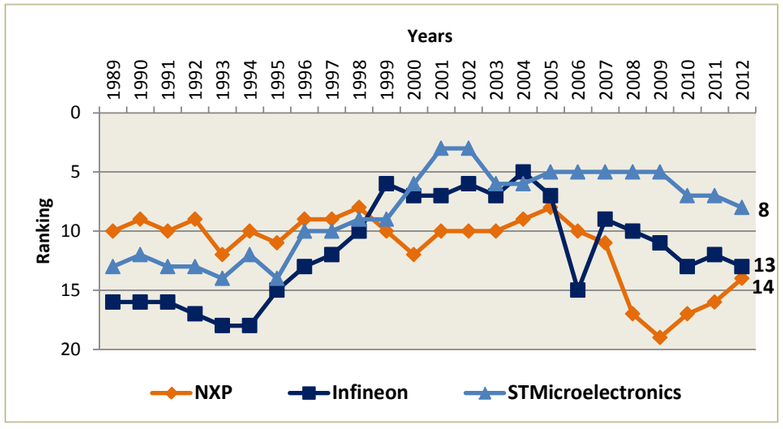
Fig. 1.14: Long term ranking of top ten semiconductor companies



Source: IHS iSuppli March 2012.

Over the last five years, the main European IDMs have pursued more focused strategies based on their strengths. Such an approach has allowed them to attain a more solid economic position, even if their ranking situation has deteriorated at worldwide level.

Fig. 1.15: Europe's contributors in semiconductors



Up to 2005: Dataquest, 2006-2012 iSuppli.

The table below (Table 1.16) delivers a detailed listing of world's top 20 semiconductor suppliers by revenue.

Table 1.16: Top 20 semiconductor supplier revenue ranking 2012

FLAG	2011 Rank	2012 Rank	COMPANY	2011 Revenue	2012 Revenue	Percent of Change	Percent of Total
	1	1	Intel Corporation	$48,721	$47,543	-2.4%	15.7%
	2	2	Samsung Electronics*	$28,563	$30,474	6.7%	10.1%
	6	3	Qualcomm	$10,198	$12,976	27.2%	4.3%
	3	4	Texas Instruments	$13,967	$12,008	-14.0%	4.0%
	4	5	Toshiba	$12,729	$10,996	-13.6%	3.6%
	5	6	Renesas Electronics	$10,648	$9,430	-11.4%	3.1%
	8	7	SK Hynix	$9,293	$8,462	-8.9%	2.8%
	7	8	STMicroelectronics	$9,735	$8,453	-13.2%	2.8%
	10	9	Broadcom	$7,160	$7,840	9.5%	2.6%
	9	10	Micron Technology	$7,365	$6,955	-5.6%	2.3%
	13	11	Sony	$5,015	$6,025	20.1%	2.0%
	11	12	Advanced Micro Devices (AMD)	$6,436	$5,300	-17.7%	1.7%
	12	13	Infineon Technologies	$5,312	$4,826	-9.1%	1.6%
	16	14	NXP	$3,831	$4,096	6.9%	1.4%
	17	15	nVidia	$3,608	$3,923	8.7%	1.3%
	14	16	Freescale Semiconductor	$4,408	$3,775	-14.4%	1.2%
	21	17	Media Tek	$3,309	$3,472	4.9%	1.1%
	15	18	Elpida Memory	$3,887	$3,414	-12.2%	1.1%
	22	19	ROHM Semiconductor	$3,267	$3,170	-3.0%	1.0%
	19	20	Marvell Technology	$3,393	$3,113	-8.3%	1.0%
All Other Companies				$109,360	$106,768	-2.4%	35.2%
TOTAL SEMICONDUCTOR				$310,205	$303,019	-2.3%	100.0%

* Significant impact on growth due to Samsung Electronics acquisition of Samsung Electro-Mechanic's 50% share of Samsung LED.

Source: IHS iSuppli Research December 2012.

In relation to the world-market, since 2001 the European market share has dropped by more than 40% (21.7% -> 11.5%). It is forecasted that for the next couple of years, the present European level in the market will be kept.

Table 1.17: Europe's semiconductor market share and share of its key-players

REGION	2001	2003	2005	2007	2009	2010	2011	2012
WORLD*	139.0	166.9	227.4	255.6	226.3	298.3	299.5	290.0
EUROPE*	30.2	32.5	39.3	40.9	29.9	38.1	37.4	33.4
E as %	21.7	19.5	17.3	16.0	13.2	12.8	12.5	11.5
European share % in Top 20	10.2	10.4	9.6	9.6	7.0	6.8	6.1	5.8

* WSTS

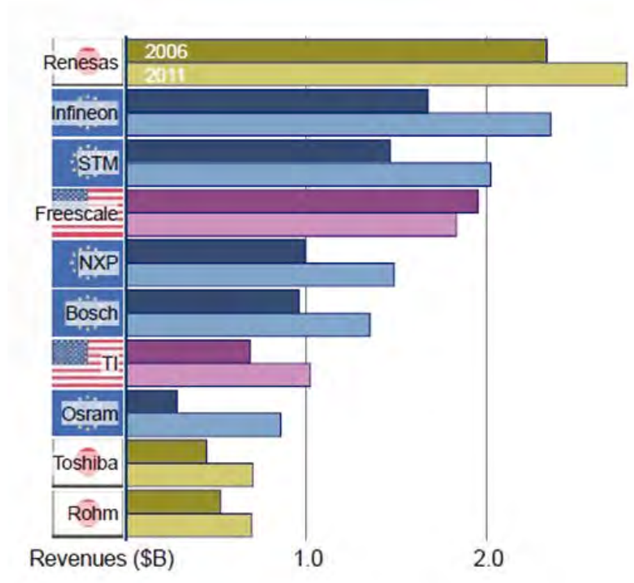
** IHS iSuppli: Research, December 2012

Since 2007, Europe's champions in semiconductors (out of WW Top 20) have lost nearly 40% of their European market share (9.6% -> 5.8%) - partially caused by strategic decisions to sell parts of their business. However, at the same time, due to the focussing of efforts on their key business, European key-players have gained leadership in quite some essential domains, like automotive, energy, security, etc.

In order to value the strategic decisions and their impact, it is important to highlight the areas where European semiconductor companies are leaders. As mentioned earlier, the automotive sector is one of these areas.

The presence, in Europe, of both leading car manufacturers and a leading electronics system industry allows for strong cooperation resulting in the achievement of a top position of Europe at the world level. Accordingly, 5 of the top 10 automotive semiconductor suppliers are European companies.

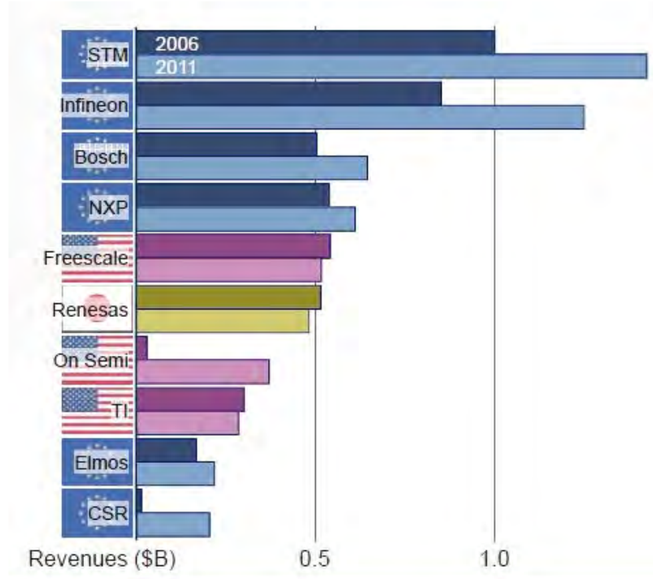
Fig. 1.18: Top 10 automotive semiconductor suppliers (2006/2011)



Source WSTS, IHS, ECCA ESIA

In 2011, six of the top ten automotive ASIC/ASSP suppliers were European representing 63% of the worldwide market.

Fig. 1.19: Top 10 automotive ASIC and ASSP suppliers (2006/2011)



Source WSTS, IHS, ECCA ESIA

Other leadership situations exist in Europe in the industrial field and in the area of equipment and material manufacturers. Since the year 2000, ASML has climbed up the top ten ladder to take the number 1 position in 2011. In 2012, ASML fell back to the number 2 position behind Applied Materials. The European firm ASMI maintained a spot in the top ten ranking in 2012 in 10th position.

Table 1.20: Top 10 equipment and material firms (1980/2012)

Rank	1980	1985	1990	1995	2000	2005	2011	2012
1	Perkin Elmer	Perkin Elmer	TEL	Applied	Applied	Applied	ASML	Applied
2	GCA	TEL	Nikon	TEL	TEL	TEL	Applied	ASML
3	Applied	G Signal	Applied	Nikon	Nikon	ASML	TEL	TEL
4	Fairchild	Varian	Advantest	Canon	Teradyne	KLA-Tencor	KLA-Tencor	LAM
5	Varian	Teradyne	Canon	LAM	ASML	Advantest	LAM	KLA-Tencor
6	Teradyne	Eaton	Hitachi	Advantest	KLA-Tencor	Nikon	Dainippon	Advantest
7	Eaton	Schlumberger	G Signal	Hitachi	Advantest	LAM	Nikon	Dainippon
8	G Signal	Advantest	Varian	Teradyne	LAM	Novellus	Advantest	Nikon
9	K&S	Applied	Teradyne	Dainippon	Canon	Canon	ASMI	Hitachi
10	Takeda Riken	GCA	SVG	Varian	Dainippon	Dainippon	Novellus	ASMI

Source Future Horizons, IMEC, 2012 VLSI Research

4. Conclusions

Thanks to various cooperative programmes like CATRENE, the status of technology in Europe is up to date at the worldwide level. On the other hand, the fact that semiconductor consumption in Europe and European semiconductor supply to the world market are both constantly declining in the last years (European consumption was 12.5% of the total world consumption in 2011 and this has moved down to 11.5% in 2012) cannot be ignored. At the same time, in 2011, 9% of the world demand for semiconductors was supplied by European companies in comparison to 8% in 2012.

The AENEAS and CATRENE Boards have identified urgent strategic actions necessary to secure the future of Europe's nanoelectronics ecosystem. These actions are twofold including (1) an increased effort supported by Industry compared to the past and (2) a request to the Member States as well as the European Union for a commitment to increase their investment on innovation compared to the past and to create favourable framework conditions. This is consistent with the recommendations delivered by the HLG for the KETs and reflects the continuous penetration of Information Technology in many domains where the enabling role is implicit.

These recommendations have been shared in a positioning document entitled Innovation for the future of Europe: Nanoelectronics beyond 2020 released in November 2012.

Highlighting the need for Europe to substantially increase its research and innovation efforts in nanoelectronics in order to maintain its worldwide competitiveness, the document outlines a proposal by companies and institutes within Europe's nanoelectronics ecosystem to invest 100 billion € up to the year 2020 on an ambitious research and innovation programme, planned and implemented in close cooperation with the European Union and the Member States.

Follow up actions, including discussions with Member States and the European Commission, have been launched by AENEAS and CATRENE with regards to the proposals made in the positioning document.

Chapter 2

CATRENE STEERING GROUPS

1. Introduction

This Chapter describes the progress and the status of the CATRENE Application and Technologies projects over the year 2012.

Status of 5th call (launched in 2012) as of 2S 2012

	POs received	FPs submitted	Projects labelled	Projects started
5th Call	Applications			
	5 --> 5 requested to submit	3*	3	2
	Technologies			
	3 --> 1 rejected, 2 requested to submit FPs	2	2	0

*2 consortia who submitted POs decided not to continue with a FP due to a negative funding outlook.

Summary of other project related news in 2012

In the Application area:

- 5 of the 7 labelled 4th Call application projects started in 2012:
  - SHARP,
  - H-INCEPTION,
  - APPSGATE,
  - NewP@ss,
  - EM4EM.
- As of 2S 2012, 16 CATRENE application projects were active out of 29 projects labelled over the 5 Calls of CATRENE. 9 projects were cancelled.
- 4 application projects from the 1st Call ended during 2012:
  - COMCAS,
  - HiDRaLoN,
  - PANAMA,
  - HERTZ.
- The Steering Group Applications carried out 12 project reviews and assessed 14 change requests.

In the Technology area:

- The 3 labelled 4th Call technologies projects started during the second semester of 2012:
  - DYNAMIC-ULP,
  - 3DFF
  - MASTER_3D.
- As of 2S 2012, 12 CATRENE technologies projects were active out of 20 projects labelled over the 5 Calls of CATRENE. 3 projects were cancelled.
- 4 technologies projects from 1st Call ended during 2012:
  - EXEPT,
  - TOETS,
  - 3DIM3,
  - PASTEUR.
- 1 technologies project from 2nd Call ended during 2012:
  - REFINED.
- The Steering Group Technologies carried out 12 project reviews and assessed 16 Change Requests.

2. The CATRENE landscape: applications and technologies objectives

CATRENE's global objectives in the field of micro/nanoelectronics shall be achieved through early leadership in most advanced System-on-chip (SoC) and System-in-package (SiP) applications, comprising of the development of architectures and standards, Intellectual Property (IP) libraries and tools, hardware-dependent software design, hardware-software co-design methodologies and finally, demonstrators for the validation of results. In this respect, the activities address the following main work areas:

- Communication and digital lifestyle,
- Safety and security including trusted platforms and secure applications,
- Automotive and transportation including environmental protection and industrial applications,
- Health and the ageing society,
- Energy efficiency, design technology (including architectures and EDA),
- Semiconductor process integration,
- Equipment, materials and manufacturing.

CATRENE projects are selected with a view to achieving pre-competitive standards and platforms in key electronic market segments thus enabling system houses to carry out necessary R&D for their own system solutions and thereby differentiating them from the competition.

With the introduction of new generations of System-on-chip (SoC) in nanoelectronics technologies, the production cost, time-to-market and volume-to-market become more and more critical on top of the need for best-in-class level of quality and reliability. The SoC approach, still widely based on the usage of cell libraries or reusable IP blocks, brings with it extreme complexity, which will further explode through future multi-core implementations in networking on chip (NoC) solutions. Accurate system level knowledge and level of validation on silicon of each block of library/IP used within new chips becomes mandatory in order to secure first silicon success. In this context, knowledge sharing between designers at all levels of co-operative projects plays a key role in cost optimisation and time-to-volume reduction, assuming that there is a constant improvement in cost-quality ratio. Thus, SoC design is and will become even more important in the CATRENE Applications area.

The so called design gap exists between what process technologies offer and the fact that with the ever increasing complexity of designs, designers are not adequately able to exploit them within reasonable design times. Moving to technology nodes beyond 65 nm causes all design steps from specification down to fabrication not only to become seriously interdependent but also directly linked to the IC's yield and reliability. In addition to the digital and analogue mixed signal design flows More than Moore requires multiphysics design flows. As a consequence, the Steering Group Applications and the Steering Group Technologies have an additional and increasingly important

objective of fostering leading edge Electronic Design Automation (EDA) methodologies and tools, which should help to overcome obstacles related to complexity and new physical phenomena.

The programme also covers the technology platforms for next generation of CMOS process, for process options and for heterogeneous systems. The integrated solutions cover not only the chip design but starting from simulations the whole board/system design including the metrology, the test, the characterisation, the failure analysis and the reliability. It includes the low cost solutions for die and package stacking, 3D integration using through silicon via or other technologies for parallel interconnections between dice. The sensors, actuators, bio-chips, fluidics, photonic are now combined on SoC or SiP. The smart sensor and actuator systems are one of the most powerful enabling technologies and require mastering several cross cutting technologies. CATRENE leading edge technology projects are essential building blocks in the nano-electronics landscape. Hence there is no one technology or process covering strictly each application fields but rather a set of processes based on silicon encompassing heterogeneous options.

In the equipment and silicon technology part, CATRENE Technologies follows the pace of the ITRS, which requests development of new equipment, new materials and new advanced substrates.

The trends towards faster introduction of options, volumes and yields for more and more sophisticated technologies place high demands on manufacturing tools and methodologies. This requires the development in parallel of the processes for an efficient and agile manufacturing solution.

3. Steering groups operation

The Steering Groups promote project proposals in line with the stringent criteria for project labelling, taking care that a proper balance exists between the specified application and technology areas in the sub-programmes.

The progress of the projects is monitored on a regular basis by members of the Steering Groups who act as reviewers and provide recommendations, at the same time. A Change Request is often necessary during the course of a project as a result of altered project conditions. Once a Change Request has been submitted, it is evaluated by the respective Steering Group. On a case-by-case basis, Change Requests are accepted directly or, forwarded to the CATRENE Support Group for further confirmation prior to acceptance.

In addition, the Steering Groups within the CATRENE Programmes often motivate large and small European companies, research institutes and universities to join their skills and forces in co-operative actions. The Steering Groups can influence the definition and selection of projects, performed by industry and academia in a way that a strategic approach is supported.

4. Steering groups composition

Steering Group Applications:

During the first semester of the year 2012:

- Mr. Luigi Grasso (Bull) left the Steering Group. Bull will look for a successor;
- Mr. Bruno Foucher (EADS) replaced Mrs. Nadine Buard (EADS);
- Mr. Thomas Scheiter (Siemens) and Christian Sebeke (Bosch) announced their resignation from the Steering Group Applications and will inform the office about their successors;
- In August Mr. José Luis Conesa (ADD) left the Steering Group in August because ADD changed the PPP policy after having taken over by an American company. In December he joined the Steering Group again working for AlphaSIP after discussion with AlphaSIP and the Spanish PA. He is representing again the Spanish participants in CATRENE;
- In November Mr. Georg Menges (NXP) replaced Mr. Peter Zegers (NXP).

Steering Group Technologies:

- Mr Timothy Robson (ST-Ericsson) left the SG-T in February 2012 and has been replaced by Dr. Torkel Anrborg (ST-Ericsson) in September;
- The Support Group agreed the replacement of the Technologies Programme Director, Mr. Michel Burle (ST Microelectronics) by Mr. Denis Rousset (STMicroelectronics). This change has been effective in September 2012.

5. Initiatives led by the CATRENE steering groups

CATRENE Design Technology Conference

The CATRENE Design Technology Conference was held in June, in Grenoble, with more than 70 participants. This was carried out in conjunction with the LETI Annual Review housed by MINATEC, Grenoble, France.

Keynotes included:

- HPC-cloud computing,
- Challenges for Embedded SW Integration: Challenges in embedded Software for industrial applications,
- Increased importance of power-devices,
- More than Moore,
- Market outlook Analyst.

In addition, the conference covered the following technical sessions:

- Multiphysics design flow,
- Test innovation,
- Embedded MPSoC Architecture,
- Smart Energy.

The second day closed with a panel session: SME Key contributors in Design flow.

EDA Roadmap

The European Roadmap for Design Automation in semiconductor products (formerly known as the MEDEA+ EDA Roadmap) is a publication produce by CATRENE which focuses mainly on “System on a Chip” (SoC) and “System in a Package” (SiP) products, taking the best of technology capabilities for addressing new markets.

The last edition, published in 2009, mainly focuses on demonstrating a complete top-down design flow, starting at specifications, then System Level Design linking designers to formal customer’s specifications, parametrisable IPs creation, standards and Design for Manufacturability (DfM) supported by new TCAD (Technology CAD) developments.

With 6 editions of the EDA Roadmap, CATRENE is committed to maintaining the document. The latest

version is available for download on the CATRENE web site http://www.catrene.org

3D Workshops

Based on an initiative of CATRENE, two 3D workshops of European co-operative projects have been organized on February 2012 in Frankfurt and November 2012 during European Nanoelectronics Forum 2012 in Munich.

The participants from ENIAC JU, FP7 and CATRENE projects expressed clear interest in continuing this fruitful experience.

This disruptive challenge/opportunity concerns the incremental usage of 3D/heterogeneous integration platform in order to decrease the CoO (Cost of Ownership) versus full 2D integration on SOC. Several running projects aim at developing new solutions both for the technology and design. In order to keep the leading edge on Heterogeneous Integration, European actors have to accelerate innovation and the promotion of European co-operative projects.

Applications review

A. PROGRAMME COVERAGE (Application projects)

1. Overview of projects

Table 2.0

Call #	Project Number	Acronym	Work Area	Status
1	CA101	PANAMA	Communication & Digital Lifestyles	Ended 30/09/12
1	CA102	PAAM	Communication & Digital Lifestyles	Cancelled 18/05/09
1	CA103	HERTZ	Communication & Digital Lifestyles	Ended 30/09/12
1	CA301	HiDRaLoN	Automotive and Transport	Ended 15/06/12
1	CA303	OTIMISE	Automotive and Transport	Started 02/07/09
1	CA304	GoldenGates	Automotive and Transport	Cancelled 23/06/09
1	CA305	PROSE	Automotive and Transport	Cancelled 22/09/09
1	CA501	COMCAS	Energy Efficiency	Ended 29/02/12
2	CA104	COBRA	Communication & Digital Lifestyles	Started 01/01/10
2	CA201	TS-CIMoNHet	Safety and Security	Cancelled 14/12/10
2	CA202	eGo	Safety and Security	Started 01/07/10
2	CA401	NIGHTINGALE	Health and the Ageing Society	Cancelled 28/05/10
2	CA402	THOR	Health and the Ageing Society	Started 01/10/10
2	CA502	SEEL	Energy Efficiency	Started 01/11/10
2	CA602	HOMEDIA	Devices and systems for digital entertainment	Cancelled 04/06/10
3	CA308	ICAF	Automotive and Transport	Started 01/10/11
3	CA403	RELY	Health and the Ageing Society	Started 01/05/11
3	CA503	OpenESL	Energy Efficiency	Cancelled 21/02/12
3	CA504	PiMSA	Energy Efficiency	Cancelled 02/03/11
4	CA109	SHARP	Communication & Digital Lifestyles	Started 01/09/12
4	CA110	AppsGate	Communication & Digital Lifestyles	Started 01/09/12
4	CA111	Ultra HD-4U	Communication & Digital Lifestyles	Labelled, Not Yet Started
4	CA206	NewP@ss	Safety and Security	Started 01/07/12
4	CA310	EM4EM	Automotive and Transport	Started 01/07/12
4	CA701	H-Inception	Design Technologies	Started 01/12/12
4	CA702	MultiSoC	Design Technologies	Cancelled 09/10/12
5	CA112	HARP	Communication & Digital Lifestyles	Started 01/01/13
5	CA505	BENEFIC	Energy Efficiency	Started 01/01/13
5	CA703	OpenES	Design Technologies	Labelled, Not Yet Started

B. CONFERENCES, PUBLISHING ACTIVITIES, PATENTS

By the end of the first semester of 2012, CATRENE Applications project consortia initiated many dissemination activities. To name a few: Participation in international conferences, publication of papers, contributions to and organisation of workshops and the filing of numerous patents.

C. APPLICATION TRENDS

Intelligent traffic systems

(NXP Semiconductors, Infineon Technologies)

Introduction

One of the main challenges in the future is lowering carbon dioxide (CO_2) emission. Nearly 30% of the energy consumption in Germany is caused by private and public transportation. In the last years the industry has provided a huge effort in research and innovation to reduce emission and energy consumption for future road vehicles significantly. So has VW recently demonstrated the first 1-liter vehicle and nearly every OEM has an electrical vehicle in the portfolio by today.

In the last few years the ultimate goal of most car manufacturers has been to complete a fully electric vehicle, protecting the environment from emissions and noise, with alternative on-board energy sources (solar) and connection to the grid. In the course of this development, a tremendous amount new innovative solutions has been created. Hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEVs), and fully electric vehicles (EVs) are only a few of the targeted and partly realized innovations. However, the cost and hence the price for customers for such cars is still very high and their operating distance limited.

Further challenges lie in future traffic volume and resulting noise, pollution, traffic jams and number of accidents. As urban population expands and city roads become increasingly congested, city planners need to come up with comprehensive urban development and innovative transport policies to address a deep-seated social and demographic change. Only in Germany there are 54,5 million vehicles registered (01.01.2013), a 1,3% increase to 2012. Also truck mileage has increased in Germany by roughly 4% according to last reports. 40% of traffic jams in Germany are caused by high volume traffic. In 2011, a German driver statistically was caught up about 36 hours in a traffic jam.

To solve those mobility challenges it is mandatory to have a strong focus on “intelligent traffic systems”. Having an integrated, intelligent traffic management system implemented …

- energy consumption can be reduced,
- operating range of EVs can be extended,
- traffic jam can be reduced,
- accidents may be avoided,
- driving becomes more convenient,
- new services can be established.

However, to achieve this ambitious goal thorough investigation, many new technology domains is mandatory.

Intelligent traffic systems

In the world’s megacities, traffic infrastructure often looks like it is collapsing under the weight of exploding population growth. Congested roads, traffic noise, the risk of accidents and general stress are all part of our daily urban lives. Intelligent traffic management and efficient public transport systems will be required to ensure the future of mobility in such crowded urban areas and to reduce energy consumption needed for mobility and transportation. Chips for urban mobility solutions aim to ensure mobility in the smart cities of the future and will reduce energy consumption, particularly petrol, in addition.

Despite double-tier multi-lane freeways, multi-hour traffic jams are an everyday scene in Peking or Shanghai. And every week some 10,000 vehicles are newly registered to join the queues. Ironically, the more mobile the population becomes, the more slowly people can expect to get where they want to go. Consequently, metropolitan areas worldwide are searching for sustainable infrastructures and mobility concepts. Authorities in many cities in Asia have realized that simply constructing more roads, tunnels or overpasses cannot relieve major traffic junctions of their daily load. Thus municipalities are forced to develop new concepts for efficient traffic management in both private and public transportation for a sustainable infrastructure.

In Asia public authorities have recognized that simply more construction will not generate the necessary relief. In many of the Asian megacities, governments seeing the rapid population growth start to react. Introducing systems for inner city tolls to control traffic flow, putting higher taxes on new cars or simply limiting car use depending on the individual number plate, those in charge are trying to gain back control.

Furthermore city councils have started to cooperate with industrial partners developing new systems to make management of individual traffic and public transport more effective.

Networked traffic systems should broaden the horizon from the focus on the ‘pure’ reduction of energy consumption towards a more holistic view on future sustainable traffic solutions in Automotive, Railway, Aviation and Shipping. Effective traffic systems must meet multiple objectives:

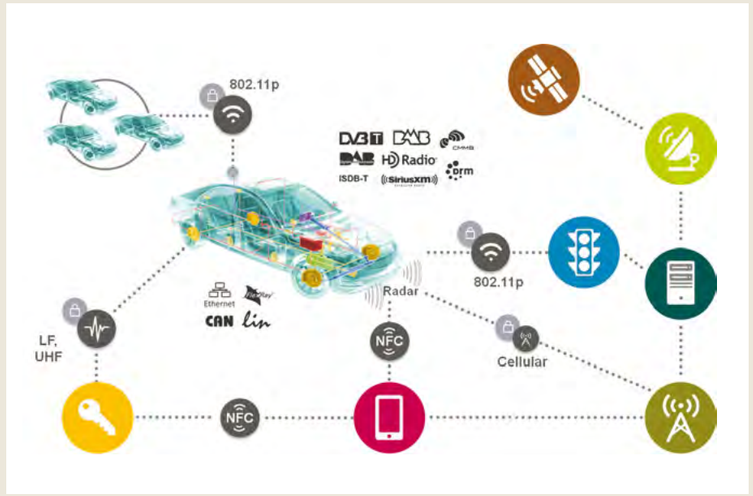
- Reduce energy consumption for the individual user and the overall system,
- Reduce unneeded congested roads,
- Reduce noise and pollution caused by combustion engines,
- Maintain the mobility that drives economic development,
- Integrate all different modes of transport: pedestrians, bicycles, motorcycles, cars and public transport.

(source: Siemens)

Closed networked transportation systems are supporting unobstructed road traffic in cities by producing as less environmental impact as possible. These intelligent traffic systems are reducing traffic noise, air pollution and energy consumption of vehicles by providing a predictive driving strategy and forward-looking operating strategies respectively increasing the operating range of EVs. By reducing stops at e.g. traffic lights or tollbooths, an optimized traffic routing that avoids congested areas and a closer co-operation between rail, tram, bus, parking and other service operators, energy consumption can be reduced up to 20%.

Besides guiding the driver for an optimized traffic flow, intelligent, connected traffic systems help to avoid dangerous traffic situations by getting information from all traffic participants. Such intelligent traffic systems may be the first step towards a comprehensive traffic control making possible a synchronization of public and private traffic flows.

The connected Car
Car to Car - Car to infrastructure - Car to portable



(source: NXP Semiconductors)

Intelligent traffic systems should be considered as multimodal and also covering trustworthy communication systems. This aims to introduce at a higher level efficiency, prediction and reliability in traffic and transportation by using data from different sources as GSM, UMTS, GPS, WLAN, DSRC, navigation systems, vehicle-to-vehicle communication, vehicle to infrastructure and others. Distributed sensor networks, communicating through RF and broadband info-busses have to be analyzed according to their deployment in Automotive & Transport. Appropriate multi-access/multi standard gateways for seamless interaction with other domains have to be developed.

High Priority Research Areas:

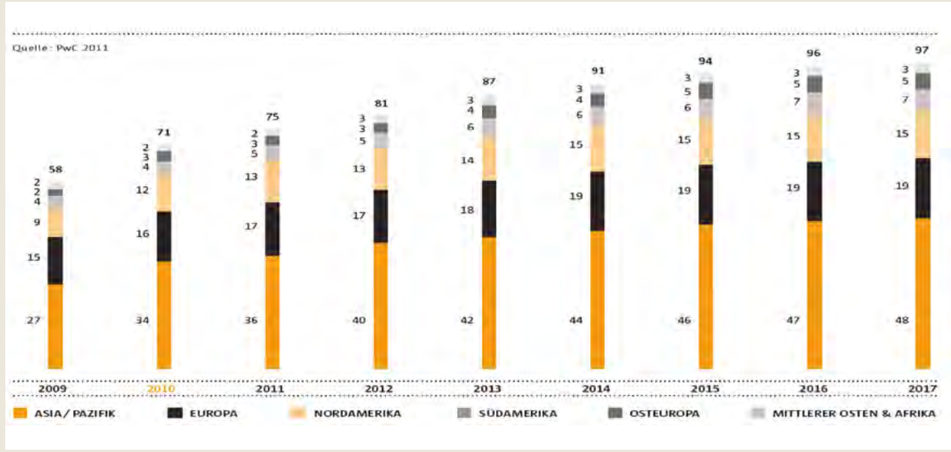
- prediction of traffic and driving situation,
- networked sensors covering the whole environment,
- intelligent traffic flow management covering efficient use of energy resources and time,
- real-time-traffic-information by using the cars as moving sensors,
- appropriate multi-access/ multi standard communication gateways,
- high performance “In-Vehicle Networking” (up to 100 Mbit/s),
- intelligent high performance data processing,
- intelligent electronics for security and privacy protection,
- concepts and introduction of pro-active communication (e.g. for e-cars: accidents, road blocks, dangerous situations, availability of charging stations, active route planning).

By bringing together city planner, city administrations, service providers, car manufacturers and technology providers integrated concepts for a future concept of an intelligent traffic systems, integrating individual and public transportation can be developed and realized. This innovation is significantly driven by innovations in the European micro- and nanoelectronics industry. The focus on e-mobility will persist, however integrated in an overall strategy.

Market:

In the EU, 6 of the world largest car manufacturers are located, producing roughly 20 million vehicles every year. In addition, Europe is also home of the world’s leading automotive electronic semiconductor and system suppliers. The European automotive semiconductor suppliers represent more than 30% of the world market.

Car production
WW 2009 – 2017



(source: PwC 2011)

Vehicles in Europe are currently fitted in average with semiconductors worth around 300 €, whereupon the semiconductor content in hybrid and electric vehicles is more than the double. Future intelligent traffic systems will increase the semiconductor content again. Ethernet, environmental sensors, LED Lighting systems, battery management systems, communication components for car to car and car to infastructure, security features for tolling and intelligent, adaptive human interfaces will need innovative semiconductor technologies and solutions. To foster the needed innovation and assure reliability at acceptable cost, nanoelectronics are the key enabler for intelligent traffic systems.

Average Semiconductor Content per Vehicle ($)

(source: Strategy Analytics July 2012)

However intelligent traffic systems are not limited to the individual car traffic. Cities are growing and in the meantime 50% of the world's population living in cities. The need for unobstructed urban and inter-city transport has never been greater. Road and rail networks are the arteries that keep the heart of our modern society beating.

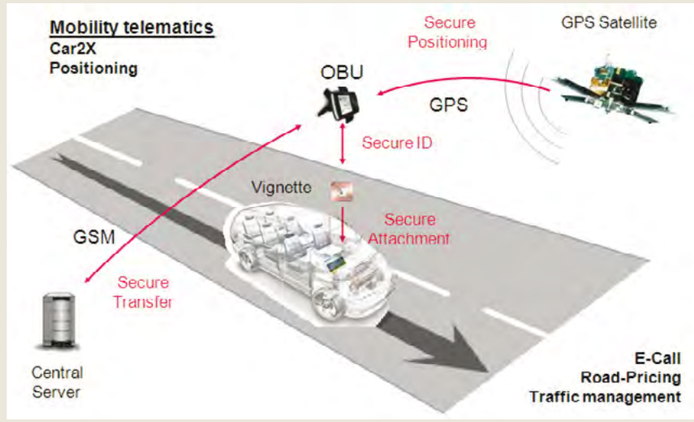
Integration and interoperability at every level of the transport system are key to smooth, continuous traffic operations and enhanced safety and security. Thanks to integrated, secure and safe solutions, all critical data can be centralised. Seamless communication systems, automatic train/bus control technologies, traffic surveillance and real-time passenger information are necessary tools for intelligent traffic systems. These technologies enable a more frequent, reliable and user-friendly, public transportation system, while faster throughput and shorter lead times generate significant gains in profitability.

Vehicles that can see and think

Intelligent automobiles can master today's traffic problems. Cars that "think" can take a load off the driver, by figuratively "taking the wheel", for instance when it comes to choosing the right route or driving in an energy-efficient manner. This intelligence is facilitated by networking systems in the car and by extending this network wirelessly to the infrastructure. Telematics Onboard-units give vehicles the capability to interact and exchange information with their environment, including for car-to-car and car-to-infrastructure communication.

(source: NXP Semiconductors)

Networking solutions of this kind can enable traffic lights and vehicles to "talk" to one another and regulate the flow of traffic. Traffic lights would tell drivers the right speed to drive through the city in order to minimize the number of red lights they have to stop at. Obstacles such as construction sites, traffic backups or other danger spots would be reported to drivers so that they can adapt their route. Public transportation buses would receive priority through a traffic management system with telematics and car to car communication enabling them to maintain better schedule reliability. Field trials are already in progress worldwide, for example in Singapore since 2010.



(source: NXP Semiconductors)

The car analyzes road conditions in real time and chooses the best route. This results in reduced fuel consumption hence in decreased CO_2 readings. In Europe field trials take place to use this type of telematic solution for road tolling. The GPS receiver determines the car's position. The distance driven is then communicated to a server over the mobile network. Finally the road toll is charged according to the real distances covered. By this pay-as-you-drive approach today's tax systems could be replaced by a more just solution. This would also allow increasing tolls during rush hour or for highly frequented roads.

An according trial in the Netherlands has demonstrated that drivers will be optimizing their route and avoid rush hours and back roads. This technology has the potential to reduce congestion by more than 50%.

E-ticketing

Public local transport agencies in China's megacities like Beijing, Wuhan, Shanghai and Hong Kong are already utilizing modern chip systems as an answer to the daily onrush of commuters. With electronic ticketing, passengers buy their virtual tickets without a long queue by using a transport card or, in the future, by using an NFC-enabled cell phone. These electronic chips are able to securely transmit data to a reader over short distances of a few centimeters – within milliseconds. At begin and the end of the journey the cell phone is swiped over the terminal and payment is done automatically. With e-ticketing used in more than 130 major cities Chinas is leading the way. But also more and more transport agencies in Europe are following the example and start NFC pilots.

NFC ticketing

(source: NXP Semiconductors)

E-ticketing however is just a first step towards implementing a new vision in traffic and transportation for smart cities. From a technical point of view, it is already possible for a cell phone to combine in one electronic device the functions of an identity card, driver‘s license, credit card and various keys, including home, car or hotel keys, as the Google Wallet already proves. This makes urban mobility concepts imaginable in which the cell phone, as a densely integrated communication platform, selects the optimum kind of transport. A destination chosen by cell phone navigation can be approached, depending on the traffic situation, by public transport, taxi or car-sharing rental. The cell phone acts as the means of payment for a bus ticket and taxi charge or even opens the door of a shared rental car parked nearby, conveniently authenticating the driver with its credentials securely stored in a secure element.

In such a mobile vision above mentioned technology enables implementing a variety of applications that simplify and improve urban mobility. Asian smart cities have a pioneering role to play here. In this smart urban mobility vision, the car is no longer the classical status symbol of the past, but the convenience of a cities’ resident. Without lengthy planning, the most efficient means of transport can be chosen and paid, guiding the way to a paradigm shift that benefits both residents as well as municipalities of smart cities.

Car sharing: driver authentication

Over all, electronic, secure ticketing and tag technology gets travellers through the barriers faster while enabling closer co-operation between operators. A similar system improves traffic flow on toll highways, tunnels and bridges. Search aids, access control systems and electronic ticketing for car parks make the smoother and more convenient. Taxis and car sharing systems require localization, maintenance and surveillance tools. Innovative sensors and communication interfaces will solve this problem.Emergency cars, fire trucks, public buses, taxis, e-vehicles and/or car-sharing systems may get a priority circuit depending on its status and the allowance to enter restricted or partly restricted areas as e.g. the inner city circle.

(source: NXP Semiconductors)

All these features will be integrated in an intelligent traffic system. For the user and the society this means:

- Fewer accidents. The US ministry of transport predicts a reduction of 80% of deadly traffic accidents.
- A reduction of the energy consumption in the area of 3 to 5% by 2020.
- A CO_2-reduction. The improved traffic flow avoids traffic jam and detours that goes along with a 10% CO_2-reduction.
- An intelligent traffic system improves service and transport frequency of the public transportation system, what improves attractiveness and acceptance.
- Economic growth: Market researchers estimate ww a 48 billion U$ market size.

The European industry is in a clear leadership concerning automotive electronics that enables the next step towards a holistic approach on Intelligent Traffic Systems for improved safety, for vehicles and road users, efficient traffic flow and low energy consumption. The strong position of the European industry in nanoelectronics and embedded technology will be a major enabler for the breakthrough of this technology and therefore strengthening the European economy.

Technologies review

A. PROGRAMME COVERAGE (Technology projects)

1. Overview of projects

Table 2.1

Call #	Project Number	Acronym	Work Area	Status
1	CT105	3DIM3	Design Technology	Ended 31/12/12
1	CT201	PRESTO	Semiconductor Process and Integration	Cancelled 31/12/09
1	CT202	STR	Semiconductor Process and Integration	Cancelled 31/12/09
1	CT204	PASTEUR	Semiconductor Process and Integration	Ended 31/12/12
1	CT301	EXEPT	Equipment, Materials and Manufacturing	Ended 31/12/12
1	CT302	TOETS	Equipment, Materials and Manufacturing	Ended 31/12/12
2	CT205	REFINED	Semiconductor Process and Integration	Ended 31/12/12
2	CT206	UTTERMOST	Semiconductor Process and Integration	Started 01/06/10
2	CT207	COCOA	Semiconductor Process and Integration	Started 01/07/10
3	CT208	REACHING 22	Semiconductor Process and Integration	Started 01/04/11
3	CT209	RF2THZ SISOC	Semiconductor Process and Integration	Started 01/07/11
3	CT210	DYNAMIC-ULP	Semiconductor Process and Integration	Started 01/01/12
3	CT305	SOI 450	Equipment, Materials and Manufacturing	Started 01/11/11
3	CT306	NGC 450	Equipment, Materials and Manufacturing	Started 01/11/11
3	CT307	EYE	Equipment, Materials and Manufacturing	Cancelled 16/03/11
3	CT402	9D-SENSE	Equipment, Materials and Manufacturing	Started 01/10/11
4	CT213	3DFF	Semiconductor Process and Integration	Started 01/05/12
4	CT312	MASTER 3D	Equipment, Materials and Manufacturing	Started 01/12/12
5	CT214	EuroProFILS	Semiconductor Process and Integration	Labelled, Not Yet Started
5	CT315	EmPower	Equipment, Materials and Manufacturing	Labelled, Not Yet Started

B. CONFERENCES, PUBLISHING ACTIVITIES, PATENTS

Dissemination of project related research and its results by CATRENE partners and consortia at international conferences or in papers is increasing with the maturity of the program and the quantity and quality of its outcome.

C. TECHNOLOGY TRENDS

How will the Mobile shape the CMOS technology?

Author: Denis Rousset, CATRENE Office

Silicon technology development has been shaped primarily by the need to continuously increase the performance of digital transistors. In line with Gordon Moore's observation, transistors have continually become cheaper, smaller, faster.

The need to get the "service on demand" without any delay is completely changing the ranking of priorities. The so-called user experience is requesting that services are accessible while people are moving. The Key Performance Indicators to be leader on the market are changing since the smartphones, tablets and others portable devices are present in our daily activities.

A rapidly growing mobile market is changing the dynamics within the silicon landscape in the post-PC era. Smaller system footprint and ultra-lower power will be the key factors for success after the just higher transistor performance. Considering the System on Chip (SoC) there is variety of IP blocks that are used to independently deliver functionality. The integration of disparate functional IP blocks on a chip urges also aggressively scaling interconnect density. This is opening the door to all "More Than Moore" technologies.

In 2012, VLSI symposium took a hard look at the future of CMOS chip technology and concluded that its future course depends on mobile applications. In this consideration a car is nothing else than a mobile device that must be always connected for the comfort of the driver and passengers.

The IDMs and Foundries semiconductor manufacturing industry is being redefined as the CPU takes a backseat to the mobile SoC.

Let's give some examples of well-known companies having a strategic involvement towards Mobile Market. Google is known to have developed the Android operating system to challenge Apple Inc. in wireless handsets. The acquisition of Motorola Mobility has recently led the company even deeper into the electronics hardware market. Today this position allows launching two hardware devices, including a tablet PC and media player.

The Consumer Electronics Show held every year in Las Vegas came to a close on January 2013. Every year the event draws crowds from around the world and highlights everything from high tech TV's to robots. Mobile phones were all the buzz. Samsung stole the show with its Galaxy Note 2. High tech video recording devices, including stop motion and time lapse cameras also made a showing. Intel showcased its new microprocessor lines which are to be used in smartphones and laptops. LG awed audiences with its amazing 3D television display. It is hard to boil down a list of what was most interesting at CES 2013.

Samsung Electronics joined other chip makers, including Intel and Qualcomm, at the 2013 Consumer Electronics Show in unveiling upcoming products for mobile devices. In Samsung's case, it was the Exynos5 Octa, an eight-core processor designed to give devices the right balance between performance and energy efficiency. The chip, introduced January 9 during the final keynote presentation of CES, leverages ARM Holdings' big. Little architecture that was first talked about in 2011. In the case of Samsung's chip, the Exynos5 Octa will have four cores based on ARM's Cortex-A15 CPU, which can handle the more compute-intensive workloads. At the same time, the chip also will house four cores based on the lower-power Cortex-A7 ARM architecture, which will handle lighter workloads and boost the chips' energy efficiency.

ST-Ericsson's FD-SOI NovaThor integrated processor/modem attracted a great deal of interest at CES where it was shown as a demo earlier this year. Thanks to the insertion of the ultra-thin buried oxide substrate, FD-SOI brings a number of fundamental improvements in the transistor electrical characteristics, while using planar manufacturing technology. From a microprocessor design perspective the advantages of FD-SOI versus bulk are cooler, faster and simpler. The processor can operate at lower voltages with still very respectable frequencies (1GHz at 0.65V). In low power modes, the FD-SOI relative advantages become more spectacular, reaching up to 100% higher frequency versus equivalent bulk low power modes. The ~35% increased efficiency at high frequencies is already more than enough for a FD-SOI dual-processors to outperform slower bulk quad-processors in the vast majority of the use cases, due to the currently limited software scalability.

Concurrently, the industry is also approaching the limits of technology scaling itself. Eventually, making transistors smaller will result in diminishing returns on key metrics like performance, power and cost. That will signify another inflection point when in the words of Gordon Moore, "making things smaller won't help anymore." The Current CATRENE projects are fully in line with the above evolutions.

Chapter 3

CATRENE CUMMULATIVE RESULTS

A. CUMULATIVE PROJECT TABLE

The Cumulative Project Table provides information on projects in terms of:

Label date: the date on which an accepted Full Proposal (FP) is awarded a CATRENE label.

Planned start date: the date on which cooperation starts as laid down in the accepted FP. Possible subsequent CRs having an impact on the winding-up period of the project do not affect this date.

Actual start date: the date on which the cooperation actually started.

Planned end date: the date on which cooperation ended as laid down in the accepted FP. Possible CRs with impact on the project's duration do not affect this date.

Actual end date: the date on which cooperation actually ended.

Table 3.0: Project data of CATRENE

Project		Label date	Planned start date	Actual start date	Planned end date	Actual/Exp. end date
CA101	PANAMA	2008-09-30	2008-10-01	2009-01-01	2011-12-31	2012-09-30
CA103	HERTZ	2009-04-22	2009-07-01	2009-10-01	2012-06-30	2012-09-30
CA301	HiDRaLoN	2008-09-30	2009-01-01	2009-03-01	2011-12-31	2012-06-30
CA303	OPTIMISE	2008-12-16	2009-06-01	2009-07-01	2013-05-30	2013-06-30
CA501	COMCAS	2008-09-30	2009-01-01	2009-03-01	2011-12-31	2012-02-29
CT204	PASTEUR	2009-04-22	2009-07-01	2009-07-01	2012-06-30	2012-09-30
CT105	3DIM3	2008-09-30	2009-01-01	2009-07-01	2011-12-31	2012-12-31
CT301	EXEPT	2008-09-30	2008-10-01	2009-02-01	2011-09-30	2012-06-30
CT302	TOETS	2008-09-30	2009-01-01	2009-03-01	2011-12-31	2012-03-01
Call 1 # ended projects per 2S 2012						**8**
CA104	COBRA	2009-12-16	2010-01-01	2010-01-01	2012-12-31	2013-04-30
CA202	eGo	2009-10-15	2010-01-01	2010-07-01	2012-12-31	2013-12-31
CA402	THOR	2009-10-15	2010-07-01	2010-10-01	2013-06-30	2014-03-31
CA502	SEEL	2009-10-15	2010-04-01	2010-11-01	2013-03-31	2013-10-31
CT205	REFINED	2009-10-15	2010-01-01	2010-01-01	2012-12-31	2012-12-31
CT206	UTTERMOST	2009-10-15	2010-01-01	2010-01-01	2012-12-31	2013-05-31
CT207	COCOA	2009-10-15	2010-01-01	2010-07-01	2012-12-31	2013-06-30
Call 2 # ended projects per 2S 2012						**1**
CA308	ICAF	2010-06-30	2011-01-01	2011-10-01	2013-12-31	2014-09-30
CA402	RELY	2010-06-30	2011-01-01	2011-05-01	2013-12-31	2014-04-30
CT208	REACHING 22	2010-10-13	2011-01-01	2011-04-01	2013-12-31	2014-03-31
CT209	RF2THZ SISOC	2010-10-13	2011-01-03	2011-07-01	2013-12-31	2014-12-31
CT305	SOI 450	2010-10-13	2011-10-01	2011-11-01	2014-06-30	2014-12-31
CT306	NGC 450	2010-10-13	2011-10-01	2011-11-01	2014-09-30	2014-12-31
CT402	9D-Sense	2010-06-30	2011-01-01	2011-10-01	2013-12-31	2014-10-31
Call 3 # ended projects per 2S 2012						**0**
CA109	SHARP	2011-09-06	2011-09-01	2012-09-01	2014-08-30	2014-08-30
CA110	APPSGATE	2011-10-12	2012-01-01	2012-09-01	2014-06-30	2015-02-28
CA111	ULTRAHD-4U	2011-06-29	2012-01-01		2014-12-31	2014-12-31
CA206	NewP@ss	2011-06-29	2012-02-01	2012-07-01	2015-01-31	2015-01-31
CA310	EM4EM	2011-10-12	2012-01-01	2012-07-01	2014-12-31	2014-12-31
CA701	H-INCEPTION	2011-10-12	2012-01-01	2012-12-01	2014-12-31	2014-12-31
CT210	DYNAMIC-ULP	2011-06-29	2012-01-01	2012-01-01	2014-12-31	2014-12-31
CT213	3DFF	2011-10-12	2012-01-01	2012-05-01	2014-12-31	2014-12-31
CT312	MASTER_3D	2011-06-29	2012-01-01	2012-12-01	2014-12-31	2015-11-30
Call 4 # ended projects per 2S 2012						**0**
CA112	HARP	2012-06-27	2013-01-01		2015-12-31	2015-12-31
CA505	BENEFIC	2012-10-12	2013-01-01	2013-01-01	2015-12-31	
CA703	OpenES	2012-10-12	2013-01-01		2015-12-31	
CT214	EuroProFILS	2012-10-17	2013-01-01		2015-12-31	
CT315	EmPower					
Call 5 # ended projects per 2S 2012						**0**

B. CUMULATIVE TECHNICAL RESULTS

1. STEERING GROUP APPLICATIONS

Ended projects:

2012:

CA101: PANAMA

The PANAMA project started officially on 01 January 2009. It had been extended in France till end of September 2012, and extended too in Belgium till end of August 2012. The Dutch partners finished their contribution to the project end of December 2011. The final review done in October 2012 concluded that the project was successfully completed.

The initial goals are achieved or surpassed. All these achievements have been disseminated through a numerous number of publications and workshops. The most innovative have been patented. And finally, industrial partners have started the exploitation of PANAMA results.

CA103: HERTZ

The HERTZ projected started on 01 October 2009 and ended 30 September 2012.

Strong collaboration on joint architecture and demonstrators can be recognised as well as knowledge exchange on application of latest sensor and network technologies. Strong vision of future home networking from application partners to semiconductor industry. Partners have started to commercialize products, have stepped up on standardisation, and are forming alliances.

CA301: HiDRaLoN

This project will lead to a number of societal benefits: Higher efficiency and less error in medical diagnostics i.e. a change from treatment to prevention; enhanced experience for TV viewers by unprecedented image quality; an additional pair of "automatic" eyes on the road; greater visibility in a dark environment, i.e. improved recognition capabilities; improved safety and flexibility of assembly lines to safeguarding man and machine.

The main objectives of the project have been achieved. All deliverables have been finished.

The project shows a long list of publications and 6 patents have been filed. Contribution to EMVA1288 standardization for High Dynamic Range sensors (inversion 4.0 the standard will be extended to nonlinear and HDR cameras) and Time of Flight (study group has been started). Prototypes of full imager chips Medical, Broadcast, Time-of-Flight, Machine Vision are functional, evaluated and achieve expected results or even surpass them.

CA501: COMCAS

Aims at breakthrough low-power design solutions for (data) communication-centric heterogeneous multi-core architectures targeting 45 nm and 32 nm CMOS technologies. These architectures will be exploited in a number of future applications.

Fields of Application generated by this ecosystem may be also rich and varied which can create a sum of new Products, Solutions or e-Services for worldwide customers. In this context the market perspective provided by technological progress in Low-Power Techniques for multi-core architecture are strategic and promising to develop any mobile embedded devices. All R&D efforts (cell library, components, methodology, tools development, …) have been deployed into our Demonstrator. Thanks to developments performed, the industrial partners consolidate market share. Overall breakthrough innovations successful consolidate the partner's position in this very competitive and aggressive market. In addition, now, the partners explore and attack new markets segments.

Active projects:

CA104: COBRA

This report refers to Full Proposal V8 (October 2012) and concerns the period 2010-2012, which was the initial time frame of the project, with 3 participating countries: France, Spain and The Netherlands. This being said, the current report corresponds to 93% of all COBRA activities. Remaining 7% will be addressed in 2013 by Spain and The Netherlands, (France concluded its works at the end of 2012). Please note that P2012 (Platform 2012) developed by ST and CEA is now renamed STHORM. The main result of the project is the whole development (until demonstration) of an open, flexible, and high performance platform based on a regular array of processors running in parallel.

2nd call Project started 01 January 2010.

CA110: AppsGate (Applications Gateway)

The project has officially started on 01 September 2012, with the Belgian and French Public Authorities officially funding the project, although the funding process was not complete in the other partner countries.

Shortly after, the German and Dutch partners have left because they have been denied funding. Then, the Spanish cluster has been strengthened with the addition of SIMON TECH to defend its case in front of the Spanish Public Authorities. Even to this date, the Spanish and Turkish partners are not officially funded.

The project is in start-up phase.

4th call Project started 01 September 2012.

CA202: eGo

The project has been in "cruise" mode during the whole period and progressed well in this last reporting period. The most significant results achieved during the period concern in particular the finalization of requirements for all applications, as well as significant progress in the development of libraries, sensors (including biometric sensors) and silicon components (BCC, Smart-Card Chip and UWB chip) that will be needed for the demonstrators.

2nd call Project started 01 July 2010.

CA206: NewP@ass

Globally, the project started with a slow ramp-up on 01 July 2012, as some partners got their final contracts later than expected after the positive feedback from the PAs. It was in particular difficult to get final confirmation of funding for all partners from France, while the Spanish partners had to withdraw and Hungarian partner could not make a national application in 2012.

This half year period enabled nevertheless, to achieve tangible results which show that the project is now on a good way to reach his full momentum.

4th call Project started 01 July 2012.

CA303: OPTIMISE

All the work packages have started technical works and four of them are now completed. The specification of digital and power applications to be used all along the project is finished as well as the identification of the associated mission profiles. In a first step, partners have validated several mitigation techniques as proofs of concept on test cases. The applicability of each of these mitigations to the applications of the project has been assessed and the first and second digital vehicle tests were manufactured. The implementation of the most relevant mitigations is almost achieved for each of the defined applications.

1st call Project started 01 July 2009.

CA308: ICAF

The project is reporting that since October 2012 all partners are funded by their local public authorities; except for Belgian partner intoPIX because Wallonia does not fund CATRENE projects.

As a result of the delayed start of partner ON Semi and the delay in funding of ON Semi and EqcoLogic, the tape-out of the first silicon will be delayed. This was already discussed during the annual review, and the project will issue a Change Request in January 2013.

Despite of the delay in the first silicon it is expected that all goals of the project will still be met before the end of the project.

A first version of the SWOT/Risk Register has been written en approved.

The first annual review took place on 25 October at Deft University of Technology.

An ICAF website has been launched in October 2012.

3rd call Project started 01 October 2011.

CA310: EM4EM (ElectroMagnetic reliability and electronic systems for Electro Mobility)

No Technical Report received.

4th call Project started 01 July 2012.

CA402: THOR

Major achievements in this reporting period are:

- The issue reported at review w.r.t. AVX has been solved.
- The good performances of the gen2 prototypes already allowed ST to exploit this technology in solar application at 175°C.
- Exemplary cooperation with respect to dual phase cooling system can be recognised.

The project reports overall good technical progress. It also reports some points of attention and corrective actions.

2nd call Project started 01 October 2010.

CA403: RELY

The RELY project work focusses on two coherent directions. At first, there is the specification and definition of the use-cases and scenarios where reliability is a major issue, as well as the assessment of the results of the technical investigations within RELY.

The second working direction is the direct technical research work, developing various techniques for predicting and/or increasing the reliability at all levels of abstraction. The research here is a direct contribution and increase of the state of the art, as can be seen from the various patents, journals, keynotes and conference contributions regarding these techniques.

In the reporting period one official change request was launched and accepted by the CATRENE steering board as a minor change request: all partners' project contribution from TU Delft had to be removed due to the funding situation of the Dutch consortium.

3rd call Project started 01 May 2011.

CA502: SEEL

The SEEL project is on track. All planned deliverables are available. The 4th workshop at TU/e Eindhoven was well attended and progress on a wide variety of demonstrators was shown. Due to the fast acceleration of SSL lighting below 4000 lm, the market requirements for HID have changed. Because of this, a CR is being prepared to rescope WP2, while continuing to focus on higher lumen packages. The low power deliverable (D2.1) will be discontinued and findings reported on.

The main focus has been on the realization of the LED demo module.

Exploitation plans have been summarized. The number of publications increased significantly in 2012.

2nd call Project started 01 November 2010.

Start-up projects:

CA109: SHARP

Project is in start-up phase.

4th call Project started 01 September 2012.

CA111: Ultra HD-4U

Project has not yet started.

CA112: HARP

Project is in start-up phase.

5th call Project started 01 January 2013.

CA503: OpenES

Project has been withdrawn due to lack of funding.

CA505: BENEFIC

Project is in start-up phase.

5th call Project started 01 January 2013.

CA701: H-Inception

Project is in start-up phase.

4th call Project started 01 December 2012.

CA702: MultiSoC

Project has been withdrawn due to lack of funding.

CA703: OpenES

Project has not yet started.

2. STEERING GROUP TECHNOLOGIES

Ended projects:

2012:

CT302: TOETS

Project successfully ended on 01 March 2012.

The TOETS project had the ambition to create a breakthrough in methods and flows used during the testing considering the test as whole technology along the value chain from Design to Application. The recent evolution in microelectronics allows the semiconductor industry to create nano-scale devices integrating giga-scale complexity. A strong consortium composed of European Semiconductor industries, Academics and SMEs had gathered together their competences to successfully address this challenge.

Test is becoming a dominant factor in overall manufacturing cost. Furthermore, the semiconductor industry is extremely competitive and can only deliver the best quality and reliability levels at the lowest cost.

Impressive results have been realized in all WPs and all milestones achieved. All quantitative targets of TOETS reached. The productivity of the test has been significantly improved resulting in a drastic cost reduction. The test development lead time has also been reduced by 40%. Many test innovative solutions and productive concepts were shared between partners. The benefits for each partner are illustrated in the "TOETS success stories" document. Improvement of the quality is beneficial for the automotive and healthcare markets. The involvement of SMEs in the project was impressive. The announcement of a new company has been a direct consequence of the positive results obtained in the TOETS project. A large number of papers and contributions to workshops/conferences were reported and standardization activities were developed. A strong interest has been reported worldwide for the TOETS results. The fruitful cooperation between all TOETS partners has to be highlighted. The TOETS project is the follower of the ended MEDEA+ NANOTEST project. The TOETS project is considered as an important project opening new opportunities for other successful European cooperation. The ENIAC project "ELESIS" follows TOETS project and takes advantage of the results of TOETS project as a starting point. Most of the TOETS partners will contribute in the ELESIS project.

1st Call Project, started on 01 March 2009.

CT301: EXEPT

Project successfully ended on 30 June 2012 with an extension of one quarter to demonstrate the EUV system.

The goal of the EXEPT project was to develop technologies, tools & infrastructures components as required for high volume EUV lithography for 22 nm node and beyond. The EXEPT project was a direct follow-up of the EAGLE (2T301) project (ended in mid-2009) in which technologies for the EUV lithographic NXE: 3100 pre-production tool platforms were developed. Five countries (Belgium, France, Italy, Germany and The Netherlands) and 15 partners (7 large firms, 4 SMEs and 4 institutes) were involved.

Over the lifetime of the project, 5 Change Requests were approved. The most important were related to the funding situation. The funding situation for the French and German partners of the EXEPT project has been positively formalized in December 2010 but ASML reduced drastically his participation due to the "non" positive conclusion by the European Commission after the notification of the Dutch financial support in March 2011. ASML maintained all development with the planned resource even though some effort has been realized outside the EXEPT project. All consortium members were funded except ASML in The Netherlands, XTREME technologies in Germany and Media Lario Technologies in Italy. A quarter of extension up to September 2012 was necessary to complete the final project milestone. The EUV lighted-on for the first time during the summer 2012 in Veldhoven.

The EXEPT project was the largest MEDEA+/CATRENE project with 1,062 Persons.Years. (P.Y.) despite the ASML decrease for the 3rd year (previously the total manpower was 1328 P.Y.). The results from the EXEPT project enhanced the position of Europe and will further secure ASML world-wide leadership in the EUVL market.

In the course of the project ASML has qualified and shipped six NXE: 3100 tools and has received 10 orders for the following model, the NXE: 3300B (which technology is partly developed inside the EXEPT project). The tool-optics were based on the development of a high Numerical Aperture EUV projection lens and illumination system with a high degree of illumination setting flexibility, delivered by Zeiss to ASML. Rewarded during the Nano-electronics Forum in Dublin, the EXEPT project has contributed of the further extension of manufacturing premises not only at ASML but also at Zeiss SMT. The EXEPT project and the previous MEDEA+ projects have strongly contributed to recognize the EUV lithography as the best solution for volume production beyond 22 nm technology node. Intel, Samsung, TSMC announced a series of agreement with ASML intended to accelerate the development of 450mm wafer technology using EUV lithography.

1st Call Project, started on 01 February 2009.

CT105: 3DIM3

The projects aims at providing new system methodologies, new design tools and system architecture solutions to handle emerging 3D integration technologies for multimedia and mobile (M3) product. The 3DIM3 project has enabled the design, from system and architecture level to layout, of 3D integrated M3 products with higher performances, lower consumption smaller size/form factor at lowest cost.

The purpose of 3DIM3 project is recognized as a priority for many competitors (TSMC, Elpida, PTi and UMC).

Progress:

3DIM3 has started on 01 July 2009. The German consortium has joined the project in September 2010. The project end date shifted by 6 months (Change Request approved in December 2010). A CR received on 13 June 2012, stipulated an extension of 6 months of the Dutch consortium to complete all tasks. Consequently all 3 consortia (Dutch, French, and German) have adopted the same end date. The third and final CATRENE annual review occurred on 11 December 2012 in Regensburg at Infineon facilities. The project ended on 31 December 2012.

In February 2012, a complaint was lodged in the US disturbing the relationship between 3 partners (CADENCE, STMicroelectronics, R3 Logic France) of the project and has mainly impacted the WP2 progress. On WP2, since the complaint, quite no progress has been possible on the common 3D generic test case impacting negatively the tool interoperability. This lawsuit has stopped direct exchanges and relationships. Technical discussions related to CAD, which were not easy since the beginning of 3DIM3, have been separated. All technical data being considered as possibly very sensitive, sharing them could be considered as risky as they could be used by lawyers.

WP1, WP3, WP4, WP5: significant progresses were realized and no delays have impacted the end of the project. A first version for all the demonstrators was available at the end of the project.

Manpower spent was 252 P.Year quite in line with 261 P.Year planned.

The Flow and final models have been delivered at the end of the project date in December 2012.

1st Call Project, started on 01 July 2009.

CT204: PASTEUR

This project aimed at exploring and developing RFID-based sensor platform technology. The monitoring of the environmental conditions of perishable goods in the supply chain between production and consumer was the targeted application. The warranty of a more effectively product's quality was demonstrated with the help of an intelligent package. PASTEUR project thereby addressed the need to increase on-line knowledge on the traceability of individual products. The demand to increase the accessibility of this kind of information about fresh products for the consumer remains a challenge. Key differentiators in the technologies were developed to reach ultra-low power at extreme low cost. Solutions available in the market today either offer only temperature-monitoring or are extremely expensive and bulky, serving either high-end markets (such as pharmaceuticals) or logistic bulk management (such as large shipments).

This project has developed technology solutions for multi-market use with a main focus on the low-end (e.g. fruit, vegetables) cold supply chain (cooled transport of goods), which enable eventually item management in the near future.

Progress:

Pasteur Project has started on 01 July 2011. Four countries (Austria, Belgium, Netherlands and Spain) remain after the withdrawal of German partners during 2010.

Over the lifetime of the project 6 Change Requests have taken into account on one hand the withdrawal of some partners, the tasks reallocation among remaining partners or new comers and on the other hand technical problem issues. Consequently, the project has been extended by 3 months (last CR in April 2012) in order to complete all tasks. The end of the project occurred on December 2012. The focus has been on the design and manufacturing of both demonstrators:

1. Integrated smart sensor tag for the fruit case.
2. Integrated smart sensor package for the meat case.

The willingness of the consortium to achieve all the goals of the project was evident. The consortium has been presenting a lot of information that showed in details the technical development of every task. In many projects, information provided by experts is dedicated to other experts and is sometimes difficult to understand for non-experts without the same expertise in this field. The partners prepared a movie which is promoting the achieved result in a common sense. The exploitation plan is opening several opportunities. Even though the market did not formally materialize, a lot of exploitation proposals are paving the way to intercept it.

The final Project Review has been set on 05 December 2012 in Paris.

Manpower spent in 3 years is 155 P.Y versus 142 P.Y planned.

1st Call Project, started on 01 July 2009.

CT205: REFINED

Goals:

The REFINED project aimed at creating fully integrated technology platforms for the embedding of NVM functions in sub-90 nm CMOS technologies (process, demonstrator, and test and reliability infrastructure) and in parallel to setup low cost effective solutions for qualified technologies (150/130 nm).

The final goal was to maintain and consolidate the leadership of European companies in offering the most advanced eNVM SoC solutions worldwide. Embedded Flash technologies play a crucial role in developing reliable, high performance Microcontroller Units (MCUs) that are used in various applications including the smartcards and the automotive segment.

These applications span a wide range from high-end automotive microcontroller applications requiring large memory densities in the multi Megabyte regime to low-end applications with the need of reprogram ability in the Kilobit regime. The different industrial partners are exploring the different axes and a global comparison of the performances, costs, benefits, robustness and potential applications.

Progress:

Several Change Requests have largely modified the contents and the partners list during the first 2 years 2010 and 2011. After the withdrawal of the Dutch partners in 2010, the refocus of the eFlash technology on the 55 nm was decided by ST. The funding situation has been quite shaky during this time frame. After the termination of funding by the Saxony, the German partners withdrew in March 2011. Even if the withdrawal of Infineon impacted in a negative way the consortium inside REFINED, the cooperation between the French and Italian industrial partners has been continued. STMicroelectronics (FR and IT), Atmel (FR) and LFoundry (FR) - and research partner CEA-LETI (FR) were taking care of the development of embedded non-volatile memory in sub-90 nm CMOS. The Italian partners of the project were not funded at all.

The REFINED program was organized in 3 work packages. The first work package targets technology development. The second work package is focusing on new modules and new cell concepts. The third one concerns IP development, testing and characterization.

All milestones planned instead of 2 have been met. After the end of the project on December 2012, LFoundry will get the final prototype on February 2013 as mentioned during the final Review in ST Micro ROUSSET.

2nd Call Project, started on 01 January 2010.

Active projects:

CT206: UTTERMOST

Goals:

The main goal of the UTTERMOST project is to develop advanced process modules, and validate a design platform (design kit, models, and libraries) for reliable and manufacturable digital CMOS 32/28 nm technologies on 300 mm wafers. For the first time, 3 European companies, member of the IBM R&D ALLIANCE "ISDA" collaborate to develop the latest core digital CMOS Technology Platform and deploy the technology at design and manufacturing level in parallel. By targeting the 28 nm half node beyond the 32 nm, the UTTERMOST project, has the ambition to promote Europe at the forefront of the semiconductor industry. The realization of the design of 4 demonstrator circuits completes the prototyping phase of the project.

Progress:

The project started on 01 January 2010 in France and on 01 June 2010 in Germany. After negotiation of funding with the different PAs involved, the consortium had to shrink. Following CR1 (submitted 14 September 2010) the consortium kept only 19 partners (3 semi companies) + 2 subcontractors in 2

countries. Among the participants, Global Foundries (GF) could not obtain an agreement for funding during the 1st phase. GF has decided to remain as an unfunded participant in the consortium cancelling its own activities but still committed to supply the services negotiated with the rest of the consortium. This was the object of Change Request 2 (CR2) released to CATRENE Office in Q4/2011 and approved in February 2012. Three major milestones (out of 14 total for the project) were achieved during the S1-2012 MM5.2, MM6.1, MM7.1. Three major milestones were achieved during the S1-2012 (MM5.2, MM6.1, MM7.1) and then MM5.2 during S2-2012.

The completion of 74 deliverables has been reached, 17 more deliverables to go in S1-2013 while 3 have been delayed by 1 to 2 quarters.

The end of the project is planned by mid-2013 in France while German Partners will continue 6 months later. The French partners have supplied a CR3 where (TCS, Dolphin, ST, IMEP, ST-E) have shift some of the manpower on the remaining months. According to CR4, ALU and UoS will complete their work beyond the end date and will report directly to their national authorities in Q4/2013.

Man power consumption in 2012 at 164.52 P.Year for a budget of 157.32 P.Year keeps the overall man power in line with planned resources.

2nd Call Project, started on 01 June 2010.

CT207: COCOA

Goals:

This project aims at developing a complete mature 3D integration technology platform covering the entire range of processes required from vertical interconnects (TSV, micro bumps…) and robust bonding to innovative packaging approaches to address a wide range of products. The main objectives of this project are to achieve chip-level three-dimensional (3D) TSV integration, Wafer-to-Wafer and Die-to-Wafer bonding, and packaging of stacked circuits, in order to create a complete technological platform for high performance and cost effective 3D systems manufacturing. The main objectives of this project is to achieve chip-level Three-dimensional (3D) TSV integration, Wafer-to-Wafer and Die-to-Wafer bonding, and packaging of stacked circuits, in order to create a complete technological platform covering the existing gap between medium (104/cm²) and high density (106/cm²) technologies, including packaging of two or more stacked layers.

Progress:

The Project was labelled on 15 October 2009.

The project started on the 01 July 2010 with a modified consortium.

The technical achievements and dissemination are at the state-of-the-art level. The major milestones planned for 2012 have been achieved and some tasks were even ahead of time. The second project Review took place on 10 September 2012 in Graz (Austria).

A change request has been validated during S2-2012. Applied Materials replaced Semitool following its acquisition by Applied Materials and ST-E announced a restructuring in April and left the project. The Change Request took into account the above information and re-allocated tasks between partners and modified the dates of milestones and deliverables accordingly.

Several technical problems required additional investigations resulting in shift of some milestones up to 3 quarters mainly in WP1 and WP2. The project end date planned on June is now pushed by end of 2013. The consortium foresees to be able to complete all tasks in the extended project period.

A project website has been implemented to share documents between partners and the PCA has been signed.

Man power consumption in 2012 at 57.3 P.year for a budget of 63.4 P.year keeps the overall man power in line with planned resources.

2nd Call Project, started on 01 July 2010.

CT208: REACHING22

Goals:

The goals of REACHING 22 are to research the optimal architecture and integration for the 22/20 nm node core CMOS technology and perform an electrical proof of concept. Preliminary assessment work using FDSOI technology was done, while in parallel the necessary process modules and an SOI substrate (UTBB) for the 20 nm node are under development. Subsequently an electrical benchmark comparison will be conducted between the bulk and the FDSOI 20 nm CMOS technology architectures based on transistor performances and an initial design library evaluation mask set. The project will contribute to the European Industry reaching the 22/20 nm technology, but also strengthen the position of the European Academics in the exploration of smaller nodes and the Beyond CMOS.

Progress:

Project started on 01 April 2011 with French and Belgian partners.

A large consortium of 24 partners was assembled at the launch date by the project coordinator. Due to lack of funding in 5 countries, the consortium was reduced to 7 partners all working closely with ST by the CR1.

The project is clearly divided into two activities. One is related to 28 nm FDSOI technology evaluations in WP0 and should last for 18 months only. The other one is related to the 20 nm technology development.

After CR1 the partners don't plan to make another Change Request until the Phase 1 will be over. At the completion of WP0 at the end of Q3/2012, there will be a critical decision deciding to go for a 20 nm bulk or a 20 nm FDSOI technology. At this stage the FDSOI approach is favored by, in any case partners will make a second change request to specify their choice in due time (Q4 2012).

3rd Call Project, started on 01 April 2011.

CT209: RF2THZ SISOC

Goals:

This project aims at the establishment of silicon technology platforms for emerging Radio-Frequency, mm-wave and THz consumer applications, 77 GHz and 120 GHz automotive radars, THz Imaging and Sensing, 60 GHz wireless networking and fast downloading Rx/Tx, 100 Gbit/s optical data communications and RF wireless communication requiring High performance devices (transmitted power, consumption, integration, isolation), as well as two way satellite communication systems.

The main target is to reduce cost while maintaining/enhancing the performance of existing solutions.

Developments of two BiCMOS technologies are forecasted within the project. For ST this is a new 0.5THz 65 nm SiGe BiCMOS platform. For NXP, the starting point will be a 0.25µm SiGe/C BiCMOS technology improved to address mm-wave to THz applications.

Progress:

The project started on 01 July 2011 with French and Dutch partners. On 01 September 2011 some German partners were joining while the others have joined on 01 March 2012 according to the request of the German Public Authorities.

A CR3 has been submitted to CATRENE at the beginning of 2012 in order to introduce a new partner Axiom IC who is contributing to the execution of a Two-way satellite communication for consumer application.

A general project kick-off meeting with all partners was held on 27 March 2012. The funding has been approved for Dutch, French, German partners while decision in Belgium is still on going. The updated schedule taking into accounts the new milestones and deliverables was approved in February 2012 with a project end date on 31 December 2014.

Some activities/Tasks are delayed related to BiCMOS55 process design kit delay by 9 months. A consortium meeting took place on the 05-06 September 2012 and the first Project Review was held on 27 November in Nijmegen.

A CR4 has validated by CATRENE office in Q3/2012 concerning the Demo 4 activities in work-package 4, aligning the delays of some milestones with resources effort and defining IMS work in WP3.

Manpower spent from the beginning of the project reached 77.4 P.Year versus 113.4 P.Year planned showing a recovery after a chaotic start.

3rd Call Project, started on 01 July 2011.

CT210: DYNAMIC-ULP (High DYNAMIC range multiprocessor for Ultra Low Power mobile devices)

Goals:

DYNAMIC-ULP aims to develop advanced process modules, and validate a design platform (design kit, models, libraries) for reliable digital and memory CMOS 22/20 nm technologies on FD-SOI (Fully Depleted - Silicon on Insulator) in European manufacturing facilities (Crolles, France). For ST-Ericsson, the goal is to get an efficient design platform for use by its European product divisions. To this end, FD SOI 22/20 nm CMOS technology first demonstrator is scheduled for Q4'13 and test & analysis of DFM effects in Q2'14. The product requirement to cover a wide dynamic range from 1.1v (to enable processors to run at 3.25 GHz) down to 0.4v (for long multimedia playback) is defining the essence of this project.

Progress:

The project Kick-Off took place in Paris on 31 January 2012. Project leadership was transferred from STE-F to ST and the FP was updated from V1 to V2 in October. In front of these modifications, the consortium prepared a Change Request validated by the CATRENE Technology Steering by Q4/2012. The CR provided the rationale of the adjustment into the tasks and efforts as well as new schedule for some milestones.

Several headlines have reinforced the consortium, providing a better visibility on the potential market while competing with the INTEL FinFet's solution:

- ST, ST-Ericsson commit to SOI, says Soitec by Peter Clarke 03 December 2012;
- Geneva, 23 April 2012 – ST-Ericsson announces new strategic direction and partnership;
- Geneva – 11 June, 2012. GLOBALFOUNDRIES to produce ST's 28 nm and 20 nm FD-SOI thanks to transfer technology from ST.

The 2 steps transition toward DYNAMIC-ULP target has started with deployment of FDSOI 28 nm Design kit. This will allow partners to experiment the way to design with FDSOI. Therefore, they will be more active during the elaboration of the 20 nm specific process solutions. This way is taking advantage of the development done into REACHING22.

The PCA has been circulated and all comments have been collected from Legal department in a version which is ready to be submitted to the signature.

Two papers were presented (SOITEC), a patent was submitted (Dolphin) and a proposal for a standardized description of memories is under way (Atrenta).

About the Funding, after getting a positive agreement from VINNOVA in Sweden and from TUBITAK in Turkey, the French Partners have met the DGCIS before the notification allowed to operational status. The present report bears testimony that partners were working all year long before the decision. Manpower spent in 2012: 75.15 P.Year versus 88.0 P.Year planned

Among 16 milestones expected in 2012, 15 are reached and 1 is delayed due to lower priority. The project will be reviewed by CATRENE on 28 March 2013 (STMicroelectronics, Grenoble).

3rd Call Project, started on 01 January 2012.

CT213: 3DFF (3D FLEX FLUIDICS)

Goals:

Three Dimensions Flex Fluidics, (3DFF) aims to develop a 3D designed sensor on flexible surfaces, enabling integration into a disposable diagnostic test, ie. low cost. The goal is to develop a digital drug screening test in saliva, which is intended to be compatible with digital mobile devices and count as evidence in court, without resorting to expensive additional test in the hospital involving blood sampling. The second use of flexible chip is to detect D-dimer, substance secreted by the human body when it is experiencing a heart attack. This Digital Diagnostic of the Infarct will also be done with a disposable diagnostic test.

Progress:

Project labeled on 12 October 2011.

Project start date was announced in May 2012 and then assessed on 01 December 2012 but with Spanish Partners only.

The topic is very innovative and the Partners must continue their push to get the Project on the tracks. For the Netherlands, as soon as 2013 budget will be known, it will be time to proceed with a NFA assuming there will be a Funding budget allocated to CATRENE.

Jose Luis Conesa is the Project Manager for 3DFF replacing Laila Quiles.

A kick-off date was proposed in Q4/2012 but cannot be materialized. CATRENE is expecting to have a kick-off meeting in Q1/2013. Without positive sign by the Partners, the project would risk to be cancelled as it is already on hold since several months.

3rd Call Project, started on 01 May 2012.

CT305: SOI450 (Development of 450mm SOI substrates, related technologies and equipment).

Goals:

The goal of the project is to develop 450mm SOI substrates and related technologies in order to bring equipment and substrates at a mature level for industrialization. The project will include tool development and SOI implementation, with feasibility milestone followed by start of a pilot line. SOITEC will lead the consortium of key equipment suppliers (EVG for bonding, Mattson for RTP), supply chain suppliers, three institutes for the evaluation of tools and technologies and IC maker Intel.

Progress:

The French partners started on 01 November 2011 and the other partners on 01 January 2012. The total duration of the project is 38 months and the project end is planned on 31 December 2014. A Change Request received on February 2012 took into account the reduction of resources because German and Belgium partners (IMEC, Mattson and FHG) could not get funding and had to adapt their resources level within the project. For Austrian partner EVG, the resources reduction anticipated is not linked to a funding risk at this point but mostly to the re-evaluation of the amount of work after EEMI450 project (former 450mm

ENIAC project): alpha tool being equipped with an automation handling system.

In the first semester the main goal was to get the project started efficiently, align all partners on the general objectives and individual expectations and reach the first deliverables in the planning. The overlap with the ending phase of EEMI450 project was a structuring factor giving the right frame for European 450mm projects. The goals of this first period were reached. The technical background for the second semester was:

- A proof of concept done for SOI SmartCutTM process,
- A target specification document available
- And above all the EVG Bonding Tool installed in Soitec.

In the second semester the project entered in a more mature phase to consolidate its roadmaps and objectives. Several issues were met, such as the withdrawal of Mattson, FHG and Siltronic; but solutions in agreement with the consortium were proposed through Change Request process and validated.

Technically Siltronic withdrawal did not interrupt bulk supply as a new bulk supplier (Sumco) is being qualified. Mattson withdrawal is still a problem. Even if we do not yet know if RTP will play a role or not in the 450mm SOI process finishing steps, there is no available tool at this moment to finish in 450mm. Some contacts have been taken with G450C on different heat treatment and other RTP supplier. No availability before 2014… In the present situation an alternative solution must be proposed to characterize the wafers.

In this semester also, the Consortium Agreement was signed, the deliverables were validated in due time and the resources level were roughly in line with Full Proposal plan.

The CATRENE review was an excellent opportunity to point out some lacking elements, suggest modifications and warn on the 2013 year achievements. In particular the clarification of targeted specifications for SOI product in the frame of the project, with the updated roadmap and product life cycle aligned with 450mm ramp-up forecast and FDSOI 300mm roadmap was done in the WP1.1 accordingly to the reviewers' request.

Finally, Soitec strengthened the links with IMEC entering in E450EDL with a dissemination objective for SOI.

Manpower spent in 2012 17.6 P.Year versus 18.9 P.Year planned. French partners anticipated 0.3 P.Year for Q4 2011.

3rd Call Project, started on 01 November, 2011.

CT306: NGC450 (Development of sub modules (for process or metrology) around a wafer handling platform, dedicated to support the 450mm wafer size migration.

Goals:

NGC450 project aims to enable in Europe the development of sub modules (for process or metrology) around a wafer handling platform, dedicated to support the 450 mm wafer size migration.

The project will be conducted in 2 steps:

- Development of a wafer handling R&D robot module;
- Integration of standard base process modules into Equipment as EFEM.

The synergy between the European companies is expected to fasten the development and reduce costs by sharing the efforts as well as the risks.

The modules and equipment resulting from the above mentioned developments will be made available and valued for a worldwide utilization, upon each European partner agreement and convenience.

The developments will be driven with the objective that the technology improvements will be backward compatible with 300 mm in order to sustain the competitiveness of the Partners. "The Industry" has made major announcements to conduct and complete the 450mm transition (Intel, Samsung, TSMC, ASML, KLA-Tencor, IMEC recent papers…).

Progress:

The project started on 01 November 2011. 4 countries are participating (Austrian, French and Irish funded partners and German unfunded partners). This project is in line with the current emulation of the 450mm ecosystem.

Indeed, since the labeling of the project on October 2010, "The Industry" has made major announcements to conduct and complete the 450 mm transition (Intel, Samsung, TSMC, ASML, KLA-Tencor, IMEC recent papers…).

The set of modules resulting from NGC450 are consistent with the current projections and customers' needs. The NGC partners have a direct exploitation of results and have a chance to secure part of the market, according to their analysis of the status of the competition. The NGC project was facing some delays due to availability of results re-used from EEMI450 ENIAC project. The EEMI450 was closed in May 2012 (3 months delay versus initial date). Some tasks mainly robotic and software specifications due in S1-2012 were 3 months postponed and the mini - environment and transfer robot designs tasks due in S2-2012 will shift by 5 to 7 months but no delays are planned for the following tasks due in 2013. The end of NGC project is planned on 31 December 2014. Two consortium meetings have already taken place plus several restricted meetings and direct contacts confirm the willingness of the consortium to recover delays. A Change Request has been validated in Q4 2012 in order to take into account the reallocation of tasks between partners and the withdrawal of the development of one software module (interface A).This interface A should be done in a new 450 mm ENIAC project. The deliverables and tasks planning and resources will be modified accordingly.

Finally, the key event has been the first CATRENE review which took place in Toulouse area (France) on 13 December. The outcome of the review was positive and reviewers made some remarks which have been taken into account in the present technical report.

The main points raised were:

i) a better focus on risk assessment, especially within "WP3 integration," where no milestones were posted in between "early 2013 - Mid 2014;"

ii) Reconsider the place for integration at the LETI, now that a dissemination road map is consolidated with EEM450PR and E450EDL projects, which will be both located at the IMEC (Be).

This will lead to a new CR proposal in 2013 to secure the project and assess some risks of deviation.

The PCA between partners has been signed.

Manpower spent in 2012 14 P.Year versus 19 P.Year planned because most of the partners have put non planned resources to complete EEMI450 ENIAC project in 2012.

3rd Call Project, started on 01 November 2011.

CT402: 9D Sense (Autonomous Nine Degrees of Freedom Sensor Module)

Goals:

The project 9D-Sense aims at an autonomous integrated 9 degrees of freedom sensing module and will therefore develop technologies for sensing itself, energy harvesting, energy storage and wireless communication. The 9D sensing system consists of a 3-axis accelerometer, a 3-axis gyroscope and 3-axis

magnetometer all of which are based on Silicon wafer technology.

A small-sized and heterogeneous integrated system is addressed to enable cost competitive solutions in the fields of consumer and health care applications. Extreme energy efficient technologies will be developed and applied. Central goal is building prototypes of the sensing system as well as their testing and proof of functionality in dedicated application environment.

Progress:

The project was starting on 01 October 2011. The 9D-Sense Kick-off meeting took place on 13 October 2011 in Reutlingen, as well as the first General Project Meetings held on 01 March 2012. A second General Project Meeting was conveyed on 02 May in Dudersatdt.

The consortium is based on 11 partners belonging to 4 countries (Austria, Finland, France and Germany).

The Specification of Sensing System has been concluded in Q1 2012. The definition of the system partitioning for sensor element, energy generation, energy storage and signal processing has been iterated several times. Progress has been achieved in the fabrication technology for accelerometer, gyroscope, and magnetometers. The required technology for the fabrication of a novel µ-battery concept is still under investigation due to technical problem. The consortium proposed to overcome this difficulty with a battery collecting energy browsed by kinetic and thermal harvesters. The signal processing algorithms and calibration concepts are being studied before implementation on the hardware.

The project is entering in some update; a new Change Request is announced coming just after the approval of CR in November 2012. A delay is reported on 2 tasks concerning the M2 (Partitioning of sensing system including power distribution).

The 9D-Sense project will have an impact not only in the motion sensor market, with its 9 degrees of freedom sensing module but also in upcoming markets related to health care applications, and secure data processing currently gaining importance towards the future of the Internet of Things (IoT).

Man power consumption in 2012 at 48.7 P.Year for a budget of 55.9 P.year

3rd Call Project, started on 01 October 2011.

CT312: MASTER-3D (MAnufacturing Solutions Targerting competive European pRoduction in 3D)

Goals:

The MASTER-3D project will contribute to transform EU leadership in R&D of 3D

Integrated Circuits into 3D IC manufacturing leadership.

Manufacturing methods to maximize process robustness and yield, minimize ramp-up time, support high volume production and reduce manufacturing cost will be developed and implemented in the consortium FABs.

The activities will focus on 3D ICs with Through Silicon Vias (TSV) and Wafer Level Packaging (WLP).

Manufacturing Excellence will be addressed by:

- tool enhancements to support high yield, mass production;
- novel 3D Wafer Parametric Test, Functional and Final Test concepts;
- Characterization and in-line Metrology methods development.

3D IC yield models allow quantifying the impact of the different yield detractors will be developed and used to accelerate the learning curve.

Progress:

Project labelled on 30 June 2011. Project start occurred on 01 December 2012. The clarification of the German consortium (new comers like Infineon) has been instrumental to re-open negotiation with German public Authorities.

Their national funding application is expected by Q1/2013.

4th Call Project, started on 01 December 2012.

Start-up projects:

CT214: EuroProFILS (Micro-Fluidic Pilot Line: European Initiative for Standardization and Manufacturability of Micro-Fluidic devices)

CATRENE 5th Call Project

Goals:

The objective of the EuroProFILS project is to bring the manufacturing of medical micro-fluidic devices to the same level of maturity and industrialisation as electronics devices. These electronics devices which have been on the market for many years have benefited from the long going standardization process. Therefore they are easily integrated in the production process of many foundries.

In the scope of the project, the Partners intend to enable the micro-fluidic industry to leapfrog from a “spider assembly” phase to a “PCB-like” phase. They want to create the FCB: Fluidic Circuit Board.

Progress:

Project labeled on 19 December 2012.

CATRENE is considering this Project is fitting the heterogeneous integration chapter and opening a promising exploitation in different domain.

Spain has been very positive and the first to fund. The topic is very innovative and the Partners must continue their push to get the Project on tracks. It is recommended to get in close contact with the Public Authorities and to manage some tuning in the Consortium structure in order to get better compliance with their expectation. For the Netherlands, as soon as the 2013 budget will be known, it will be time to proceed with a NFA. For France, the consortium would make sure that further effort of some existing industrial partners will contribute to give a better confidence level to Public Authorities to decide on Funding.

The project start would be appreciated by mid-2013.

CT315: EmPower (Embedded Power components for electric vehicle applications)

CATRENE 5th Call Project

Goals:

EmPower has a clear goal to develop an innovative packaging concept for high-power modules for e-mobility and industrial applications. This concept is based on chip embedding technology for thin IGBTs and diodes and an innovative double-sided wafer plating process and equipment for thin wafers. The radical innovation of the concept lies on double-sided cooling, vertical current and heat flow in order to drastically improve heat dissipation and the thermal impedance of the embedded power cores.

Progress:

Project labeled on 19 December 2012.

This project is potentially interesting for the automotive industry with the foreseen emergence of the autonomous electric car. It is important that the Partners take care of this negotiation steps with their Public Authorities.

It will be wise to get in close contact in each country and to make a better promotion of the targeted market and to provide an exploitation forecast for each Partner.

It is very an interesting Project fitting with German priorities; the national application must be completed. It could be necessary to have better description of the Austrian exploitation before any decision. The French participation is considered as marginal; still not very clear objective in the exploitation for French partner.

CATRENE is expecting to have CT315 running before mid-2013.

Chapter 4

CATRENE PROJECT & PARTNER LISTS

A. CATRENE PROJECTS

Table 4.0: Active projects as per 2S 2012

CA104 CL2 COBRA		
ACTIVE	ACE - ASSOCIATED COMPUTER EXPERTS	NLD
	CAPS ENTREPRISE	FRA
	COMPAAN DESIGN	NLD
	ECOMUNICAT ELECTRONICS	ESP
	LETI	FRA
	LIST	FRA
	NXP	NLD
	SAPEC	ESP
	ST-ERICSSON	NLD
	STMICROELECTRONICS	FRA
	SYNOPSYS	NLD
	TEDESYS GLOBAL	ESP
	TU DELFT	NLD
	TU EINDHOVEN	NLD
	UNI BARCELONA	ESP
	UNI CANTABRIA	ESP
	VISTA-SILICON	ESP

CA109 CL4 SHARP		
ACTIVE	BILCEM	TUR
	BULL	FRA
	CEA - LETI	FRA
	DVLX - IZMIR INSTITUTE OF TECHNOLOGY	TUR
	LINERA	TUR
	LIP6	FRA
	METASYMBIOSE	FRA
	OPTISIS	TUR
	THALES	FRA

CA110 CL4 APPSGATE		
ACTIVE	4MOD TECHNOLOGY	FRA
	ARD-ALPES RECHERCHE ET DEVELOPPEMENT	FRA
	ATMEL SPAIN	ESP
	IMMOTRONIC	FRA
	INSTITUT TELECOM	FRA
	LIG LAB	FRA
	NXP	FRA
	OPTRIMA	BEL
	PACE FRANCE	FRA
	RIPPLE MOTION	FRA
	SIMON TECH	ESP
	SOFTKINETIC	BEL
	STMICROELECTRONICS	FRA
	TECHNICOLOR	FRA
	UNIVERSITY OF BARCELONA	ESP
	VESTEL	TUR
	VIDEO STREAM NETWORKS	ESP

CA202 CL2 eGo		
ACTIVE	ATOS ORIGIN WORLDLINE	FRA
	CONTINENTAL	FRA
	DECAWAVE	IRL
	GEMALTO	FRA
	IDEX	NOR
	INRIA	FRA
	INSTITUTE OF TECHNOLOGY CORK	IRL
	LINCOR SOLUTIONS	IRL
	PRECISE BIOMETRICS	SWE
	STMICROELECTRONICS	FRA
	TYNDALL INSTITUTE	IRL

CA206 CL4 NewP@ss

ACTIVE	AENA	ESP
	CEA - LETI	FRA
	COMPUWORX CORPORATION	HUN
	EVOLEO TECHNOLOGIES	PRT
	GEMALTO	FRA
	GIESECKE & DEVRIENT	DEU
	GRAZ UNIVERSITY OF TECHNOLOGY	AUT
	ID3 SEMICONDUCTORS	FRA
	INFINEON	DEU
	INFINEON	AUT
	INSTITUTO DE TELECOMUNICACOES	PRT
	IQUADRAT	ESP
	ISEN	FRA
	ITA - INSTITUTO TECNOLOGICO DE ARAGON	ESP
	NXP	AUT
	NXP	DEU
	NXP	FRA
	SIC -STIFTUNG SECURE INFOMATION & COMMUNICATION TECHNOLOGIES	AUT
	STMICROELECTRONICS	FRA

CA303 CL1 OPTIMISE

ACTIVE	AIRBUS	FRA
	ALTER	ESP
	ARQUIMEA	ESP
	ATMEL	FRA
	CEA-LETI	FRA
	CNM - CENTRO NACIONAL DE MICRO-ELECTRONICA IMB	ESP
	CONTINENTAL	FRA
	D&T MICROELECTRONICA	ESP
	EADS IW	FRA
	IMS LAB	FRA
	IROC TECHNOLOGIES	FRA
	RENAULT	FRA
	STMICROELECTRONICS	FRA
	TIMA	FRA
	UIB - UNIVERSITY OF BALEARIC ISLANDS	ESP
	UNIVERSIDAD CARLOS III MADRID	ESP
	UNIVERSITE PROVENCE	FRA
	VALEO INTERIOR CONTROLS	FRA

CA308 CL3 ICAF

ACTIVE	ADIMEC	NLD
	AXON	NLD
	EQCOLOGIC	BEL
	GRASS VALLEY	NLD
	HASSELT UNIVERSITY	BEL
	INTOPIX	BEL
	ON SEMICONDUCTOR	BEL
	TU DELFT	NLD
	UNIVERSITY OF GHENT	BEL

CA310 CL4 EM4EM

ACTIVE	APPLUS+	ESP
	AUDI	DEU
	AUSTRIAMICROSYSTEMS	AUT
	BRNO UNIVERSITY OF TECHNOLOGY	CZE
	CATENA	NLD
	CEA - LETI	FRA
	CONTI TEMIC	DEU
	DAIMLER	DEU
	ELMOS SEMICONDUCTOR	DEU
	EMC MCC	NLD
	FAU - UNIVERSITY OF ERLANGEN-NURN-BERG	DEU
	IMA - INSTITUTE OF MICROELECTRONIC APPLICATIONS	CZE
	INFINEON	DEU
	INFINEON	AUT
	LAAS - CNRS	FRA
	MELEXIS	BEL
	NEXIO	FRA
	NXP	DEU
	OKMETIC	FIN
	PHILIPS	NLD
	ROBERT BOSCH	DEU
	ROBERT BOSCH	AUT
	SEAT	ESP
	SKODA AUTO	CZE
	TU DORTMUND	DEU
	UNIVERSITAT POLITECNICA DE CATALUNYA	ESP
	UNIVERSITY OF GHENT	BEL
	UNIVERSITY OF HANNOVER	DEU
	UNIVERSITY OF TWENTE	NLD
	VALEO	FRA
	VTI TECHNOLOGIES OY	FIN
	VTT	FIN
	ZUKEN	DEU

CA402 CL2 THOR

ACTIVE	AMPERE LABS	FRA
	BRUCO	NLD
	CIRTEM	FRA
	EADS IW	FRA
	HISPANO-SUIZA	FRA
	NXP	NLD
	PHILIPS HEALTHCARE	NLD
	PRODRIVE	NLD
	SOITEC	FRA
	STMICROELECTRONIC	FRA
	THALES MICROELECTRONICS	FRA
	TPC	FRA
	TU EINDHOVEN	NLD
	UCL	BEL
	UNIVERSITY OF VERSAILLES-SAINT-QUENTIN-EN-YVELINES	FRA
	VALEO SYSTÈMES DE CONTROLE MOTEUR	FRA

CA403 CL3 RELY

ACTIVE	ATMEL	FRA
	CEA - LETI	FRA
	EADS IW	FRA
	EADS IW	DEU
	ENST	FRA
	FRAUNHOFER	DEU
	FRAUNHOFER - IISB	DEU
	INFINEON	ROU
	INTRINSIC-ID	NLD
	MUNEDA	DEU
	STMICROELECTRONICS	FRA
	TU EINDHOVEN	NLD
	TU MUNICH	DEU
	UHB - UNIVERSITY OF BREMEN	DEU
	X-FAB SEMICONDUCTOR FOUNDRIES	DEU

CA502 CL2 SEEL

ACTIVE	AUDI	DEU
	BAG ELECTRONICS	DEU
	BENDER + WIRTH	DEU
	BE SEMICONDUCTOR INDUSTRIES	NLD
	BIC INDUSTRIES	NLD
	DCD TECHNOLOGY	NLD
	ELMOS	DEU
	FRAUNHOFER IZM	DEU
	INFINEON	DEU
	LETI	FRA
	MODULAR LIGHTING	BEL
	NXP	DEU
	NXP	NLD
	OSRAM	DEU
	PHILIPS	DEU
	PHILIPS	BEL
	PHILIPS	FRA
	PHILIPS LIGHTING	NLD
	PHILIPS RESEARCH	NLD
	RUHR - UNI BOCHUM	DEU
	TU DELFT	NLD
	TU EINDHOVEN	NLD
	ULIS	FRA
	VALEO VISION	FRA

CA505 CL5 BENEFIC

ACTIVE	ATRENTA	FRA
	CEA	FRA
	CEA-LETI	FRA
	CTTC	ESP
	FRAUNHOFER	DEU
	GSLDA	PRT
	IMEC	NLD
	INSTITUTO DE TELECOMUNICACOES	PRT
	IQUADRAT	ESP
	LEAT / CNRS - UNIVERSITE DE NICE SOPHIA ANTIPOLIS	FRA
	N.A.T.	DEU
	NXP	NLD
	RECORE SYSTEMS	NLD
	SIGNALION	DEU
	ST-ERICSSON	FRA
	ST-ERICSSON	NLD
	STMICROELECTRONICS	FRA
	SYNOPSYS	NLD
	THALES	FRA
	THALES	ESP
	TIMA	FRA
	TU BERLIN	DEU
	TU DELFT	NLD
	TU EINDHOVEN	NLD
	TU VALENCIA	ESP
	UCLM	ESP

CA701 CL4 H-INCEPTION

ACTIVE	ATRENTA	FRA
	BRIO APPS ALPHASIP	ESP
	CONTINENTAL AUTOMOTIVE	FRA
	COVENTOR	FRA
	CPE LYON	FRA
	DIZAN-SYNC	NLD
	FRAUNHOFER	DEU
	MAGILLEM DESIGN SERVICES	FRA
	NORTHROP GRUMMAN LITEF	DEU
	NXP	AUT
	NXP	DEU
	NXP	NLD
	REDEN	NLD
	ROBERT BOSCH	DEU
	ST-ERICSSON	FRA
	STMICROELECTRONICS	FRA
	TU DELFT	NLD
	TWT	DEU
	UNI VIENNA-ICT	AUT
	UPMC / LIP-6	FRA

CT206 CL2 UTTERMOST

ACTIVE	ALCATEL-LUCENT	DEU
	CAMECA	FRA
	CEA - LETI	FRA
	CEMES	FRA
	DOLPHIN INTEGRATION	FRA
	FRAUNHOFER	DEU
	IBS - ION BEAM SERVICES	FRA
	IMEP	FRA
	INTEL MOBIEL COMMUNICATIONS	DEU
	INTEL MOBIEL COMMUNICATIONS	FRA
	LTM	FRA
	SERMA	FRA
	ST-ERICSSON	FRA
	STMICROELECTRONICS	FRA
	THALES	FRA
	UNI STUTTGART	DEU

CT207 CL2 COCOA

ACTIVE	AIT - AUSTRIAN INSTITUTE OF TECHNOLOGY	AUT
	ASM BELGIUM	BEL
	AMS	AUT
	APPLIED MATERIALS	FRA
	BESI	AUT
	EV GROUP	AUT
	IM2NP	FRA
	LETI	FRA
	SPTS - SPP PROCESS TECHNOLOGY SYSTEMS	GBR
	ST-ERICSSON	FRA
	STMICROELECTRONICS	FRA
	UNI VIENNA / EMST	AUT

CT208 CL3 REACHING 22

ACTIVE	CEA - LETI	FRA
	IMEP/INPG	FRA
	LTM/CNRS	FRA
	ST-ERICSSON FRANCE	FRA
	STMICROELECTRONICS	FRA
	SOITEC	FRA
	UCL - CATHOLIC UNIVERSITY OF LOUVAIN	BEL

CT209 CL3 RF2THZ SISOC

ACTIVE	AGILENT TECHNOLOGIES	DEU
	ASTRA	LUX
	ASTUS	FRA
	BRUCO INTEGRATED CIRCUITS	NLD
	CEA - LETI	FRA
	IEMN	FRA
	IES - INSTITUT D'ELECTRONIQUE DU SUD	FRA
	IHP - INNOVATION FOR HIGH PERFORMANCE MICROELECTRONICS	DEU
	IMS	FRA
	MASER ENGINEERING	NLD
	MICRAM MICROELECTRONIC	DEU
	NXP	FRA
	NXP	NLD
	ROBERT BOSCH	DEU
	SALLAND ENGINEERING	NLD
	SILICON RADAR	DEU
	STMICROELECTRONICS	FRA
	SYNVIEW	DEU
	TU BERLIN	DEU
	TU DRESDEN	DEU

CT210 CL4 DYNAMIC-ULP

ACTIVE	ACREO	SWE
	ATRENTA	FRA
	CEA - LETI	FRA
	DOLPHIN INTEGRATION	FRA
	ERICSSON TURKEY	TUR
	INFINISCALE	FRA
	SOITEC	FRA
	ST-ERICSSON	FRA
	ST-ERICSSON	SWE
	STMICROELECTRONICS	FRA
	UCL - CATHOLIC UNIVERSITY OF LOUVAIN	BEL

CT305 CL3 SOI450

ACTIVE	AVP ADIXEN	FRA
	ALTATECH	FRA
	ASM	NLD
	CEA - LETI	FRA
	EV GROUP	AUT
	IMEC	BEL
	INTEL	IRL
	SOITEC	FRA

CT306 CL3 NGC450

ACTIVE	AIS AUTOMATION DRESDEN	DEU
	ASYS	DEU
	CEA - LETI	FRA
	EV GROUP	AUT
	FRAUNHOFER	DEU
	HAP	DEU
	INTEL	IRL
	RECIF TECHNOLOGIES	FRA
	SOITEC	FRA

CT312 CL4 MASTER_3D		
ACTIVE	AIR LIQUIDE ELECTRONICS SYSTEMS	FRA
	AMS	AUT
	AXO	DEU
	CAMTEK	BEL
	CAMTEK	ISR
	CEA - LETI	FRA
	CNRS-LIRMM	FRA
	DOUBLECHECK	DEU
	DR YIELD	AUT
	EV GROUP	AUT
	FHG IWMH	DEU
	FOGALE NANOTECH	FRA
	IMS	FRA
	INFINEON	DEU
	ISIS SENTRONICS	DEU
	NXP	DEU
	PVA TEPLA ANALYTICAL SYSTEMS	DEU
	QUALTERA	FRA
	ROCKWOOD WAFER RECLAIM	FRA
	SPTS TECHNOLOGIES	FRA
	STMICROELECTRONICS	FRA

CT402 CL3 9D-SENSE		
ACTIVE	AIR LIQUIDE	FRA
	AUSTRIA MICROSYSTEMS	AUT
	BOSCH SENSORTEC	DEU
	FRAUNHOFER	DEU
	GEMALTO	FRA
	HSG - IMIT	DEU
	MICROPELT	DEU
	OTTO BOCK HC	DEU
	ROBERT BOSCH	DEU
	TU-DARMSTADT	DEU
	UNIVERSITY OF HELSINKI	FIN

Table 4.1: Start-up projects as per 2S 2012

	CA111 CL4 UltraHD-4U	
START-UP	ALCATEL-LUCENT	ESP
	BARCO	BEL
	EPUN - ECOLE POLYTECHNIQUE DE L'UNIVERSITE DE NANTES	FRA
	EXTENDED SECURE TECHNOLOGIES	NDL
	HISPASAT	ESP
	I2CAT FUNDACIO	ESP
	IRDETO	NLD
	MAXX-XS	NLD
	NXP	FRA
	PACE FRANCE	FRA
	PHILIPS	BEL
	PHILIPS	NDL
	SAPEC	ESP
	STMICROELECTRONICS	FRA
	STONEROOS	NLD
	TECHNICOLOR	FRA
	THOMSON	FRA
	UNIVERSIDAD POLITÉCNICA DE MADRID	ESP
	VITEC MULTIMEDIA	FRA
	WIERICKE	NLD

CA112 CL5 HARP		
START-UP	CEA LETI	FRA
	EADS	FRA
	PROBAYES	FRA
	STMICROELECTRONICS	FRA
	SAPEC	ESP
	UNIVERSITY AUTONOMA DE BARCELONA	ESP
	UNIVERSITY OF CANTABRIA	ESP

CA703 CL5 OpenES

START-UP	CEA	FRA
	CISC SEMICONDUCTOR	AUT
	CONCEPT ENGINEERING	DEU
	DFKI BREMEN	DEU
	DOCEA POWER	FRA
	ECSI	FRA
	EVATRONIX	POL
	FRAUNHOFER	DEU
	INDRA SISTEMAS	ESP
	INFINEON	DEU
	INTEL	DEU
	LIEBHERR-ELEKTRONIK	DEU
	MAGILLEM DESIGN SERVICES	FRA
	NXP	DEU
	NXP	NLD
	OFFIS-INSTITUTE FOR INFORMATION TECHNOLOGY	DEU
	STMICROELECTRONICS	FRA
	SYNOPSYS	NLD
	THALES	FRA
	TU EINDHOVEN	NLD
	UNIVERSITAT AUTONOMA DE BARCELONA	ESP
	UNIVERSITY JOSEPH FOURIER	FRA
	UNIVERSITY OF CANTABRIA	ESP
	UNIVERSITY PADERBORN	DEU
	VECTOR FABRICS	NLD

CT213 CL4 3DFF

START-UP	ATMEL SPAIN	ESP
	ADVANCED PACKAGING CENTER - APC	NLD
	ALPHASIP	ESP
	BOSCHMAN TECHNOLOGIES	NLD
	CNM - CENTRO NACIONAL DE MICRO-ELECTRONICA	ESP
	DRÄGER	DEU
	INSTITUTO ARAGONÉS DE CIENCIAS DE LA SALUD	ESP
	LABORATOIRE DE PHOTONIQUE ET DE NANOSTRUCTURES	FRA
	MADRID MUNICIPAL POLICE -SECURITY GENERAL COORDINATION	ESP
	MICROFLUIDIC CHIPSHOP	DEU
	TU BERLIN	DEU
	TOPPAN PHOTOMASKS	FRA

CT214	CL5	EuroProFILS	
START-UP		ADVANCED LIQUID LOGIC FRANCE	FRA
		ADVANCED PACKAGING CENTER	NLD
		ALPHASIP	ESP
		APIX TECHNOLOGY	FRA
		AXXICON MOULDS EINDHOVEN	NLD
		BARTELS MIKROTECHNIK	DEU
		CEA-LETI	FRA
		CLARIANT FRANCE	FRA
		CMP	FRA
		CNM-CSIC	ESP
		ENABLINGMNT	NLD
		EVEON	FRA
		FLUIGENT	FRA
		FRAUNHOFER	DEU
		IBS-ION BEAM SERVICES	FRA
		IPDIA	FRA
		LIONIX	NLD
		MEDIMETRICS PERSONALIZED DRUG DELIVERY	NLD
		MICROFLUIDIC CHIPSHOP	DEU
		MICRONIT MICROFLUIDICS	NLD
		PHILIPS	NLD
		PHOENIX SOFTWARE	NLD
		RHODIA	FRA
		SANOFI AVENTIS	FRA
		TNO	NLD
		TOPPAN PHOTOMASKS	FRA
		UNIVERSITY OF TWENTE	NLD
		UNIVERSITY OF ZARAGOZA	ESP

CT315	CL5	EmPower	
START-UP		AT&S	AUT
		ATOTECH	DEU
		CONTI TEMIC	DEU
		STMICROELECTRONICS	FRA
		TU BERLIN	DEU
		VIENNA UNIVERSITY OF TECHNOLOGY	AUT

Table 4.2: Ended projects as per 2S 2012

CA101	CL1	PANAMA	
ENDED		AGILENT	BEL
		AMCAD	FRA
		CEA-LETI	FRA
		ELTA SYSTEMS	ISR
		ENST	FRA
		ESIEE	FRA
		IEMN	FRA
		IMS LAB	FRA
		KUL-ESAT	BEL
		MC2 TECHNOLOGIES	FRA
		NXP	FRA
		NXP	NLD
		OMP	BEL
		ST-ERICSSON	BEL
		STMICROELECTRONICS	FRA
		THALES COMMUNICATIONS	FRA
		TNO DSS	NLD
		TU DELFT	NLD
		TU EINDHOVEN	NLD

CA103	CL1	HERTZ	
ENDED		DIALOG	NLD
		DICE - DANUBE INTEGRATED CIRCUIT ENGINEERING	AUT
		INFINEON	AUT
		IQUADRAT	ESP
		PHILIPS TP VISION	NLD
		PHILIPS LIGHTING	NLD
		PHILIPS RESEARCH	NLD
		QUINTOR	NLD

CA301 CL1 HiDRaLoN

ENDED	BME VIKING	HUN
	BUDAPEST UNIVERSITY OF TECHNOLOGY AND ECONOMICs	HUN
	CRS IIMOTION	DEU
	DEUTSCHE THOMSON	DEU
	E2V SEMICONDUCTORS	FRA
	FRAUNHOFER	DEU
	GRASS VALLEY NEDERLAND	NLD
	HELION VISION	DEU
	IMS CHIPS	DEU
	LE2I	FRA
	NIKHEF	NLD
	PHILIPS HEALTHCARE	ISL
	PHILIPS HEALTHCARE	NLD
	PHILIPS	DEU
	PILZ	DEU
	THALES ANGENIEUX	FRA
	TU DELFT	NLD
	VIIMAGIC	DEU

CA501 CL1 COMCAS

ENDED	ATRENTA	FRA
	AXIOM IC	NLD
	LEAT	FRA
	LETI	FRA
	LIST	FRA
	NXP	NLD
	RECORE SYSTEMS	NLD
	ST-ERICSSON	FRA
	ST-ERICSSON	NLD
	STMICROELECTRONICS	FRA
	SYNOPSYS	NLD
	THALES COMMUNICATIONS	FRA
	TIMA	FRA
	TU DELFT	NLD

CT105 CL1 3DIM3

ENDED	CADENCE DESIGN SYSTEMS	FRA
	CASSIDIAN	FRA
	EADS	FRA
	FRAUNHOFER	DEU
	INFINEON	DEU
	LYON INSTITUTE OF NANOTECHNOLOGY	FRA
	LETI	FRA
	NXP	FRA
	NXP	NLD
	R3LOGIC	FRA
	RECORE SYSTEMS	NLD
	STMICROELECTRONICS	FRA
	SYNOPSYS	NLD
	TIMA	FRA
	TU DELFT	NLD

CT204 CL1 PASTEUR

ENDED	BOSCHMAN TECHNOLOGIES	NLD
	CNM - CENTRO NACIONAL DE MICROELECTRONICA IMB	ESP
	DSM	NLD
	IMEC	NLD
	INKOA	ESP
	KATHOLIEKE UNIVERSITEIT LEUVEN	BEL
	NTC WEIZ	AUT
	NVC - NETHERLANDS PACKAGING CENTRE	NLD
	NXP SC	AUT
	NXP SC	BEL
	NXP SC	NLD
	PHILIPS APPLIED TECHNOLOGIES	NLD
	PHILIPS CONSUMER LIFESTYLE	NLD
	PHILIPS MIPLAZA	NLD
	TNO - THE NETHERLANDS ORGANIZATION	NLD
	TU DELFT	NLD
	TU EINDHOVEN	NLD
	VERHAERT	BEL
	WAGENINGEN UR	NLD

CT205 CL2 REFINED

ENDED	ATMEL	FRA
	INFINEON	DEU
	LETI	FRA
	LFOUNDRY	FRA
	STMICROELECTRONICS	ITA
	STMICROELECTRONICS	FRA

CT301 CL1 EXEPT

ENDED	ADIXEN VACCUUM PRODUCTS	FRA
	AMTC	DEU
	ASM	BEL
	ASML	NLD
	BRUKER	DEU
	CARL ZEISS	DEU
	DIFFER	NLD
	DMS	DEU
	FRAUNHOFER IIS	DEU
	IMEC	BEL
	IMS CHIPS	DEU
	MEDIA LARIO	ITA
	PHILIPS EUV	DEU
	SAGEM DEFENSE SECURITE	FRA
	SUSS MICROTEC PHOTOMASK	DEU
	XENOCS	FRA
	XTREMETEC	DEU

CT302 CL1 TOETS

ENDED	ATMEL SPAIN	ESP
	ATMEL NANTES	FRA
	D4T SYSTEMS	NLD
	E2V SEMICONDUCTORS	FRA
	IMSE - CNM	ESP
	INESC PORTO	PRT
	INFINEON	AUT
	INFINEON	FRA
	IROC TECHNOLOGIES	FRA
	JTAG TECHNOLOGIES	NLD
	KATHOLIEKE UNIVERSITEIT LEUVEN	BEL
	LETI	FRA
	LIST	FRA
	NXP	FRA
	NXP	NLD
	OPHTIMALIA	FRA
	PHILIPS	NLD
	QSTAR TEST	BEL
	SALLAND ENGINEERING	NLD
	STMICROELECTRONICS	FRA
	SUPELEC	FRA
	TEMENTO SYSTEMS	FRA
	TIMA	FRA
	TOMORROW OPTIONS	PRT
	UNIVERSITE MONTPELLIER II	FRA
	UNI TWENTE	NLD

Chapter 5

CATRENE ORGANISATION

The Signing Members of the CATRENE programme entered into a cooperation agreement (the « CATRENE Frame Agreement, ») which came into effect on 15 May 2008.

At this time, the signatories of this cooperation agreement asked the MEDEA OFFICE Association to pursue its management and support mission for the benefit of the CATRENE programme with the evolution of some articles of the MEDEA OFFICE Association.

The evolutions of the Articles of Association mainly addressed the change of the name of the association "MEDEA Office Association" to "CATRENE Office Association," the replacement of the positions of two Vice-Chairmen by one Vice-Chairman, the change of the treasurer and some other updates in order to be in line with the needs of the new programme CATRENE. Being a simple change of denomination, without the creation of a new identity, all contracts and deeds signed with the association, under the former denomination MEDEA Office, were able to remain unchanged.

The "CATRENE Frame Agreement" ensures the conformity of the Articles of Association with new legal and regulatory provisions in force.

With ST-Ericsson having joined CATRENE as a signing member in 1S 2009, the CATRENE Board is now composed by twelve voting representatives.

CATRENE BOARD

The CATRENE Board is the top executive body for the CATRENE Organisation. It is responsible for the strategy and coherence of the whole Programme. It establishes general rules for the Programme management and it interfaces with Public Authorities for Programme strategy and co-funding. The composition of the CATRENE Board reflects on the one hand the participation of contributing industry and research institutes but also countries allied in the CATRENE programme. It is the responsability of the Board to nominate the CATRENE Chairman.

CATRENE SUPPORT GROUP

The CATRENE Board is assisted by the CATRENE Support Group. The CATRENE Support Group decides on project proposals for issuing CATRENE labels. It deals with all operational issues regarding the management of the Programme in view of the strategic objectives and available resources of CATRENE.

CATRENE SCIENTIFIC COMMITTEE

The primary objective of the Scientific Committee is to report on latest technology trends in Academia on a worldwide basis and to accomplish annual tasks defined by the Board and dedicated to the specific benefits of the European industry. To that end, the composition of the Committee is adjusted yearly to obtain optimal results.

CATRENE STEERING GROUPS

The two CATRENE Steering Groups "Applications" and "Technologies," give recommendations on strategic orientation and are responsible for the initiation of projects, their evaluation and for their monitoring.

There are companies not being part of the 12 signing members of the Frame Agreement of the CATRENE programme, that have been invited to join the activities of the Steering Groups.

CATRENE OFFICE

The CATRENE Office, located in Paris, assists the CATRENE entire organisation. It is a central contact point and a meeting place for the whole CATRENE Community. It also handles the Programme's interface with the outside world.

The table on the following page shows the present participation in the four formal CATRENE bodies (Board, Support Group, Steering Groups for Applications and Technologies).

Table 6.0: CATRENE organisation bodies

Partner	Board	Support Group	Steering Group Applications	Steering Group Technologies
Signing members				
Alcatel-Lucent	R. Fechner	*K. Schattauer*[17]	W. Templ	
ASMI	C. del Prado	H. Westendorp		B. van Nooten
ASML	E. Meurice	R. Hartman		G. Alberga
Bull	M. Guillemet	J-F. Lavignon	[3]	
CASSIDIAN (EADS)	J-P. Quemard	H. Mokrani	B. Foucher[12]	
Carl Zeiss	W. Kaiser[13]	R. Pforr		R. Pforr
Infineon Technologies	R. Ploss	N. Lehner	H. Roedig	W. Dettmann K. Pressel
NXP Semiconductors	K. Sievers[10]	F. van Roosmalen	G. Menges[15]	D. Gravesteijn
Robert Bosch	D. Hoheisel[14]	P. van Staa	[6]	S. Lindenkreuz
ST-Ericsson	C. Ferro[5]	G. Matheron[11]		[9]
STMicroelectronics	J-M. Chery	G. Matheron	M. Diaz Nava M. Zuffada P. Blouet	M. Morelli D. Thomas
Technicolor	V. Pizzica	[2]	H. Heijnen	
Representatives of the Scientific Commitee	G. Declerck (IMEC) H. Lakner (FhG) L. Malier (LETI)			
Invited companies				
AlphaSIP			JL. Conesa[8, 16]	
Air Liquide				A. Soulet
Atmel			E. Palm[1]	C. de Prost[1]
ContiTemic Microelectronic			R. Kohl	
Gemalto			J-P. Tual	
GLOBALFOUNDRIES				W. Buchholtz
Micron Technology				L. Baldi[1]
Philips			P. Merkus	
Siemens			[7]	
Siltronic				D. Graef
Soitec				N. Kernevez
CATRENE	E. Villa (Chair) J. Dulongpont (Secr.)	E. Villa (Chair) J. Dulongpont (Secr.)	P. Koch (Secr.)	D. Rousset (Secr.)[4]

1 As permanent guest.
2 Replacement of Romenteau in SG to be nominated by Technicolor.
3 Grasso left SG-A in March 2012. No replacement announced.
4 Burle replaced by Rousset in CATRENE and SG-T in September 2012.
5 Tingaud replaced by Ferro in April 2012 in the Board.
6 Sebeke left SG-A in July 2012. No replacement announced.
7 Scheiter left SG-A in August 2012. No replacement announced.
8 Conesa left SG-A in July August. No replacement announced.
9 Robson left SG-T in February 2012. No replacement announced.
10 Penning de Vries replaced by Sievers in September 2012.
11 Rousset replaced by Matheron in September 2012.
12 Buard replaced by Foucher in May 2012 in SG-A.
13 Dorsel replaced by Kaiser in April 2012.
14 Denner replaced by Hoheisel in July 2012.
15 Zegers was replaced by Menges in October 2012.
16 Conesa returned to SG-A in December 2012.
17 Loesch retired in January 2013. Interim replacement.

Chapter 6

CATRENE COMMUNICATION

Overview

CATRENE is committed to providing the media and its stakeholders (public authorities, partner organisations including large companies, SMEs, academia and institutes) with the most accurate and timely information available related to the programme and its projects. CATRENE is also dedicating to representing and promoting the European nanoelectronic R&D community.

Accordingly, communication activities and tools have been implemented throughout the lifespan of the CATRENE programme to ensure a reliable flow of information, which include brokerage events, publications, a public website and intranet.

CATRENE corporate communication

CATRENE corporate image brochure

Online communication

CATRENE website

Programme and project information, contacts, events, partners, projects and details thereof, useful links, press clips, publications, newsroom, project calls, etc.

www.catrene.org

CATRENE intranet

Password protected internal communication for CATRENE partners and Public Authorities.

www.catrene.org

CATRENE project documents

CATRENE project result sheets

As of 2S 2012 one result sheet has been issued and 4 are in the pipeline.

CATRENE project profiles

As of 2S 2012, 21 CATRENE project profiles have been issued and 4 are in the pipeline.

CH 6

Positioning paper: Innovation for the Future of Europe: Nanoelectronics Beyond 2020

Board members of AENEAS and CATRENE presented the positioning document to Neelie Kroes, Vice-President of the European Commission on 21 November 2012 in Munich. Upon this occasion, its implementation was discussed. Further discussions have been launched in parallel with Member States.

In this picture (from left to right): Kurt Sievers - President of AENEAS, Neelie Kroes - Vice-President of the European Commission, Enrico Villa - Chairman of CATRENE

AENEAS and CATRENE have released, end of November 2012, a new positioning document entitled Innovation for the future of Europe: Nanoelectronics beyond 2020 that describes an ambitious research and innovation programme to help address societal challenges and secure the future of the European nanoelectronics industry.

Highlighting the need for Europe to substantially increase its research and innovation efforts in nanoelectronics in order to maintain its worldwide competitiveness, the document outlines a proposal by companies and institutes within Europe's nanoelectronics ecosystem to invest 100 billion € up to the year 2020 on an ambitious research and innovation programme, planned and implemented in close cooperation with the European Union and the Member States.

The document identifies urgent strategic actions necessary to achieve these goals. They include (1) an increased effort supported by Industry compared to the past and (2) a request to the Member States as well as the European Union for a commitment to increase their investment on innovation compared to the past and to create favourable framework conditions. These actions are in line with the recommendations delivered by the High Level Group (HLG) for the KETs and reflect the continuous penetration of Information and Communication Technology in many domains where the enabling role is implicit.

The positioning paper is available for download in the CATRENE public website

European Nanoelectronics Forum (ENF)

Since 2008 the European Nanoelectronics Forum is a common event organized by CATRENE, the EUREKA cluster programme, and the ENIAC Joint Undertaking. Both public-private partnerships are working in close synergy for European leadership in nanoelectronics. In 2012, the European Commission's Seventh Framework Programme (FP7) joined as co-host of the European Nanoelectronics Forum.

Informative dedicated web pages are created every year allowing people to request an invitation, register, and book their hotel room with a negotiated room rate.

Forum history

- 2001: Amsterdam
- 2002: Antwerp
- 2003: Berlin
- 2004: Paris
- 2005: Barcelona
- 2006: Monte Carlo
- 2007: Budapest
- 2008: Paris
- 2009: Noordwijk
- 2010: Madrid
- 2011: Dublin
- 2012: Munich
- **2013: Barcelona**

ENF 2012 highlights:

- More than 300 participants attended the event;
- 74 projects were showcased;
- CATRENE projects won the Exhibition Award's first three places;
- High level keynote speakers such as Neelie Kroes, Vice-President of the European Commission and Peter Bauer, Advisor to the Infineon Management Board.

ENF 2012 pictures

Plenary session

Poster & demo session

Poster & demo session

NFC technology - voting booth

2012 Innovation Award Ceremony

2012 Exhibition Award Ceremony

Common Brokerage Event (CBE)

Each year, a Common Brokerage Event is organised by AENEAS and CATRENE. It brings together the European Nanoelectronics Community, to generate ideas for project proposal and to start consortia preparations.

CBE 2013 results:

- *2 day event;*
- *More than 200 participants;*
- *8 sessions according to work area;*
- *resulting in 28 new project ideas.*

CBE 2012 pictures

Integrated power & Energy efficiency workshop hosted by the CATRENE Scientific Committee

Paris, 23 January 2013

The workshop, attended by 60 participants for across Europe, summarized the content of a new report delivered by the CATRENE Scientific Committee on Integrated Power and Energy Efficiency. The report aimed at providing the status of this domain as well as proposing orientations for future developments in Europe.

The complete report will be available by the end of February 2013.

Seen in the press

ARTICLE	SOURCE	COUNTRY	DATE (Year 2012)
Fostering innovation-led clusters	Economist Intelligence Unit	GBR	February
Le programme CATRENE	Technologies de l'information et de la communication (TIC)	FRA	23 February
AAP: 5ème appel à projets CATRENE	ARDI Rhône-Alpes	FRA	23 February
The move to 450mm: Europe's perspective	Solid State Technology	USA	03 April
Cooling down mobile devices	EUREKA	BEL	01 June
Analyse	Bits&Chips	NLD	01 October
First EUV lithography optics from Carl Zeiss	Silicon Semiconductor	GBR	29 October
Der neue Mann an Infineons Spitze	elektroniknet	DEU	31 October
Driving down road accident fatalities	EUREKA News	BEL	November
Can governments afford R&D?	ElectroniksWeekly	GBR	20 November
EU-Kommissarin Neelie Kroes verspricht Unterstützung der Chip-Industrie	elektroniknet	DEU	21 November
We must keep manufacturing in Europe, says Neelie Kroes	ElectroniksWeekly	GBR	21 November
European semis make European industry competitive, says Bauer	ElectroniksWeekly	GBR	22 November
Les prix de l'innovation Catrene-Eniac témoignent de l'avancée de la R&D européenne en production	ElectroniqueS	FRA	22 November
London Calling: Pass me that 100 billion euro note	EETimes	GBR	28 November
European nanoelectronics industry proposes to invest 100 B€ for innovation	Business Wire	GBR	28 November

ARTICLE	SOURCE	COUNTRY	DATE (Year 2012)
€100bn 'needs to be invested in European nanoelectronics'	Pera technology		29 November
Nanoélectronique : 100 milliards d'euros seraient nécessaires pour rester dans la course	ElectroniqueS	FRA	29 November
L'industrie européenne de la nanoélectronique propose d'investir 100 milliards d'€ dans l'innovation	TF1 News	FRA	December
L'industrie européenne de la nanoélectronique propose d'investir 100 milliards d'€ dans l'innovation	Business Wire	FRA	6 December
Forschungsförderung macht Computer energieeffizienter	VDI nachrichten		7 December

CATRENE
Programme Review - Excerpts Year 2012

Chapter 7

GLOSSARY OF TERMS

A. GLOSSARY OF TERMS

Abreviation	Description
ABS	Antilock Braking System
ACC	Adaptive Cruise Control
AD	Analogue / Digital
ADC	Analogue Digital Converter
ADSL	Asymmetric Digital Subscriber Line
AFE	Analogue Front End
AFEOL	Advanced Front End On-Line
AFNOR	Association Française de Normalisation
AMADEUS	Simulation Tool
AMS	Analog / Mixed-Signal
ANSI	Telecom Standardisation body (US)
ArF	Argon Fluoride
ARMC	ADSL Reference Micro-Controller
ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Signal Processor
ATM	Asynchronous Transfer Mode
ATM PON	Asynchronous Transfer Mode Passive Optical Network
ATPG	Automatic Test Pattern Generation
ATSC	Advanced Television Systems Committee
BAC	Basic Access Control (1st generation Passport)
B2B	Business to Business
B2C	Business to Customer
BCD	Bipolar –CMOS-DMOS technology
BIC	Bulk Current Injection
BE	Boundary Elements
BEOL	Back-End of Line
BGA	Ball Grid Array package
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BISR	Built-in Self Repair
BIST	Built-in Self Test
CA	Certificate Authority
CAD	Computer Aided Design
CAE	Computer Aided Engineering
CFA	Critical Feature Analysis
CAGR	Compound Annual Growth Rate
CAM	Computer Assisted Manufacturing
CAN	Controlled Area Network

Abreviation	Description
CAP	Carrier less Amplitude / Phase modulation technique
CDMA	Code Division Multiple Access
CENELEC	European Committee for Electro-technical Standardisation
CEO	Chief Executive Officer
CFD	Computational Fluid Dynamics
CISE	Circuit Sizing Environment
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
COB	Chip On Board
COF	Chip On Flex
COFDM	Orthogonal Frequency Division Multiplexing
COO	Cost of Ownership
COTS	Components of the Shelf
CPU	Central Processing Unit
CR	Change Request
CSP	Cryogenic Spectrometers
CVD	Chemical Vapour Deposition
CVE	Verification Software Tool
CWA	CEN Workshop Agreement
DA	Digital / Analogue
DAB	Digital Audio Broadcast
DAVIC	Digital Audio Visual Council
DC	Direct Current
DDB	Digital Data Broadcast
DFA	Design for Analysis
DfM	Design for Manufacturability
DfT	Design for Testability
DfY	Design for Yield
DIP	Dual In-line Package
DMC	Digital Movie Controller
DMOS	Double Diffused CMOS
DMT	Discrete Multitone modulation Technique
DMU	Digital Mock-Up
DNA	Deoxyribonucleic Acid
DRC	Design Rules Checking
DUT	Device Under Test
DRAM	Dynamic Random Access Memory
DRM	Design Rule Manual
DSLAM	Digital Subscriber Line Access Multiplexer

Abreviation	Description
DSP	Digital Signal Processing
DSPS	Digital Signal Processor Selection
DSPF	Standard file name used in parasitic data generation
DSSS	Direct Sequence Spread Spectrum
DTV	Digital Television
DUV	Deep Ultra Violet
DVB	Digital Video Broadcast
DVD	Digital Versatile Disk
EAC	Extended Access Control V1.11 (2nd Generation Passport or Residence Permit)
EAL	Evaluation Assurance Level (1 to 7)
EBDW	E-Beam Direct Write
EBU	European Broadcasting Union
ECC	European Citizenship Card
EC-SEA	European Commission – Semiconductor Equipment Assessment
EDA	Electronic Design Automation (tools)
EDGE	Enhanced Data Rate for GSM Evolutions
EDP	Electronic Data Processing
EEPROM	Electrical Erasable Programmable Read Only Memory
EGR	Exhaust Gas Re-circulation
e-HIC/EHIC	European Health Insurance Card
EM	Electro-Migration
EMC	Electro Magnetic Coupling
EMI	Electromagnetic Interference
EPCM	Enhanced Peripherals Capabilities Micro-controller
EPL	Electron Projection Lithography
EPROM	Electrical Programmable Read Only Memory
ERC	Electrical Rules Checking
ESA	European Space Agency
ESD	Electro Static Discharge
ESH	Environment Safety and Health
ESRF	European Synchrotron Research Facility
ESP	Electronic Stability Programme
ESTI	European Telecommunications Standards Institute
EUV	Extreme Ultra Violet
EWS	Electrical Wafer Sorting
FAR	False Acceptance Rate
FC	Flip-Chip
FCOB	Flip-Chip on Board

Abreviation	Description
FD	Fully Depleted
FDTD	Finite Differences in Time Domain
FE	Finite Elements
FEOL	Front End Of Line
FFT	Fast Fourier Transform
FHSS	Frequency Hopping Spread Spectrum
FIB	Focussed Ion Beam
FIB SEM	Focussed Ion Beam Scanning Electron Microscopy
FIT	Failures in Time per Megabit
FPGA	Field Programmable Gate Array
FP	Full Proposal
FRR	False Rejection Rate
FSAN	Full Service Access Network
FX	Flexible frequencies
GDP	Gross Domestic Product
GDS	Graphic Data System
GE-XRF	Grazing Emission X-Ray Fluorescence
GLASEE	Gate Level Analysis of Single Event Effect
GPL	GNU Public Licence
GPRS	Global Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
GTEM	Gigahertz TEM
HASOP	Hazard Operability
HCI	Hot Carrier Injection
HDD	Hard-Disk Drive
HDI	High Density Interconnect
HDP	High Density Packaging
HDSL	High bit-rate Digital Subscriber Line
HFC	Hybrid Fibre Coax
HIPAA	Health Insurance Portability and Accountability Act
HPC	High Pass Filter
HSCSD	High Speed Circuit Switched Data
HT	High Tension
HTML	Hyper Text Mark-up Language
HV	High Voltage
IAS	Identification, Authentification, digital Signature
IBIS	I/O BufferInformation Specification
IC	Integrated Circuit

Abreviation	Description
ICC	Integrated Circuit Card
ICAO	International Civil Aviation Organization
ICE	Information-processing Communication Entertainment
ICEM	Integrated Circuit Emission Model
ICIM	Integrated Circuit Immunity Model
ICT	Information and Communication Technologies
ICTA	Information & Communication Terminal &nd Access
IDDD	Quiescent current - under specific testing conditions
IDDQ	Quiescent current - the "switch on" current of the device
IEC	International Electro-technical Commission
IETF	Internet Engineering Task Force
IFD	Interface Device
IIH	Current I Input High
IIL	Current I Input Low
IOH	Current I Output High
IOL	Current I Output Low
I/O	Input / Output
IOP	Interoperability
IoT	Internet of Things
IOZH	Current I Output high impedance (Z) High
IOZL	Current I Output high impedance (Z) Low
IP	Intellectual Property
IP	Internet Protocol
IPL	Ion Projection Lithography
IPR	Intellectual Property Rights
IRSE	Infra Red Spectroscopic Elipsometry
ISDN	Integrated Service Digital Network
ISM	Industrial Scientific Medical band
ISMT	International Sematech
ISO/IEC	International Standard Organisation / International Electro-technical Standard Committee
ISSCC	International Solid State Circuits Conference
IST/SEA	Semiconductor Equipment Assessment Programme of the EC
IT	Information Technology
ITEA	Information Technology for European Advancement
ITRS	International Technology Roadmap for Semiconductors
ITU	International Telecommunication Union (International standards body)
IXRTT	Korean 2,5G Services Standard

Abreviation	Description
J-CDMA	Japanese Standardisation body
JTAG	Joint Test Action Group
KET	Key Enabling Technologies
KrF	Krypton Fluoride
LAN	Local Area Network
LBS	Location Based Services
LC	Low Cost
LEN	Local Entertainment Network
LMT	Linear Magnetic Tape
LNA	Low Noise Amplifier
LOCOS	Local Oxidation Of Silicon
LSF	Load Sharing Facilities
LTCC	Low-Temperature Co-fired Ceramic
LTO	Linear Tape-Open
LYS	Library Yield System
MADS	Multipurpose Antenna Design Simulator
MBPS	MegaBits Per Second
MCM	Multi Chip Module
MCP	Maturity Check Point
MCU	Micro Controller Unit
MEAC	Modular Extended Access Control
MEMS	Micro-Electro-Mechanical Systems
MHP	Multimedia Home Platform
MIM	Metal-insulation-metal
MIT	Massachusetts Institute of Technology
M2M	Machine to Machine
MMC	Multimedia Card Assoiation
MMDS	Multipoint Microwave Distribution System
MoC	Match on Card
MOM	Method of Moments
MOS	Metal Oxide Semiconductor
MoT	Match on Terminal
MPEG	Moving Pictures Experts Group
MPLS	Multi-Protocol Label Switching
MPU	Micro Processor Unit
MRAM	Magnetic Random Access Memory
MSTPG	Mixed Signal Test Program Generation
NBTI	Negative Bias Temperature
NDSA	Nippon Development Space Agency

Abreviation	Description
NFC	Near Field Communication
NGL	Next Generation Lithography
NP	Nano Photonics
NSEG	Non-Selective Epitaxi Germanium
NVM	Non Volatile Memory
OCV	On Chip Variation
OEM	Original Equipment Manufacturer
OES	Optical Emission Spectroscopy
OFDM	(System and building Block) Name of the circuit
OLT	Operating Life Tests
OMA	Open Mobile Alliance
OMTP	Open Mobile Terminal Platform
OPC	Optical Proximity Correction
OS	Operating System
OTA	Over The Air
OTP	One Time Programmable
PA	Public Authority
PACE	Passport Authenticated Connection Establishment
PASC	Passport Authenticated Secure Connection
PBTI	Positive Bias Temperature
PCB	Printed Circuit Board
PCM	Personal Cards Microreader
PD	Partially Depleted
PDA	Personal Digital Assistant
PDK	Process Development Kit
PED	Personal Electronic Device
PEEC	Partial Element Equivalent Circuit
PFC	Poly Fluor Carbon
PG	Pattern Generator (for mask making)
PIDEA	Packaging and Interconnections Development for European Applications
PKI	Public Key Infrastructure
PLL	Phase-Lock-Loop
PM	Project Manager
PMB	Project Management Board
PMD	Polarisations Modem Dispersion
PMR	Professional Mobile Radio communications
PP	Protection Profile
PO	Project Outline
PON	Passive Optical Network

Abreviation	Description
P&R	Place & Route
POTS	Plain Old Telephone Services
PPT	Party Per Trillion
PSO	Project Support Officer
PSOS	Plug-in Silicon Operating System
PSTN	Public Switched Telephone Network
PWB	Printed Wiring Board
PY	Person Years
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat Non leaded
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
R&D	Research & Development
RET	Resolution Enhancement Technique
RF	Radio Frequency
RF-EMI	Radio Frequency – Electro Magnetic Interference
RFI	Radio Frequency Interference
RTD	Research and Technology Development
RTL	Register Transfer Level
SAL	Service Access Layer
SBD	Soft Breakdown
SC	Semiconductor
SDSL	Symmetric Digital Subscriber Line
SEA	Semiconductor Equipment Assessment
SEE	Single Event Effect
SEFI	Single Event Failed Interrupt
SEM	Scanning Electron Microscope
SER	Single Event Rate
SET	Single Event Transient
SEU	Single Event Upset
SG-A	Support Group Applications
SI	Signal Integrity
SIM	Subscriber Identification Module
SIP	System in Package
SiGe	Silicon Germanium
SM	Site Manager
SME	Small and Medium Enterprises
SMS	Short Message Service
SNR	Signal to Noise Ratio

Abreviation	Description
SO	Small Outline
SOA	Silicon on Anything
SoC	System on a Chip
SOI	Silicon on Insulator
SOP	Small Outline Package
SPC	Statistical Process Control
SQFP	Shrink Quad Flat Pack
SRA	Strategic Research Agenda
SRAM	Static Random Access Memory
SSTA	Statistical Static Timing Analysis
STB	Set-top Box
STI	Shallow Trench Isolation
STM	Scanning Transmission Microscope
STXRF	Synchrotron Total Reflection X-Ray Fluorescence
SVG	Silicon Valley Group
TCAD	Technology Computer Aided
TCG	Trusted Computing Group
TDD	Time Division Duplexing
TEM	Transverse Electromagnetic
TMC DASIE	Transient Monte-Carlo Detail Analysis of Secondary Ion Effect
TNC	Trusted Network Connect
TOC	Total Oxygen Content
TOLT	Termination component for Optical Line Termination
TONU	Termination component for Network Unit
TPCA	Trusted Computing Platform Association
TPD	Trusted Personal Device
TPM	Trusted Processor Module
TSS	TCG Software Stack
TTF	Time-To-Fab
TTM	Time-To-Market
TXRF	Total Reflection X-ray fluorescence
UFB	USB Flash Device
UHF	RF > 1 GHz
UMTS	Universal Mobile Telecommunication System
UPW	Ultra Pure water
USB	Universal Standard Bus
USIM	Universal Subscriber Identification Module
USJ	Ultra Shallow Junction
UTE	Union des Techniciens de l'Electricité

Abreviation	Description
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
VDSL	Very High Speed Digital Subscriber Line
VHDL	Very High Design Language
VHDR	Very High Data Rate
VLIW	Very Long Instruction Waves
VLSI	Very Large Scale Integration
VOD	Video On Demand
VPD-TXRF	Vapour Phase Deposition – Total Reflection X-Ray Fluorescence
VRMC	VDSL Reference Micro-Controller
VSIA	Virtual Socket Interface Alliance
VSO	Very Small Outline
WAN	Wireless Area Network
WAP	Wireless Access Protocol
WCDT	Worst Case Determination Tool
WCMT	Tungsten Chemical Mechanical Polishing
WD-XRF	Wavelength Dispersive X-Ray Fluorescence
WEN	Wide Entertainment Network
WiFi	Wireless Fidelity
WiMAX	Worldwide interoperability for Microwave Access
WLAN	Wireless LAN
WLP	Wafer Level Package
WLR	Wafer-Level Reliability
WPM	Work Package Manager
xDSL	X-Digital Subscriber line
XRR	X-Ray Reflection
xTAS	World Semiconductor Trade Statistics

CATRENE

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