



# CA104 | Computing fabric for high performance applications [COBRA]

## PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	✓
Health and aging society	
Safety and security	
Energy efficiency	✓
Digital lifestyle	✓
Design technology	✓
Sensors and actuators	
Process development	
Manufacturing science	
More than Moore	
More Moore	
Technology node	

## HIGH QUALITY, HIGH SPEED USER-CENTRED COMMUNICATIONS SYSTEMS

### Partners:

ACE  
 CAPS Enterprise  
 CEA-LETI  
 CEA-LIST  
 Compaan  
 Ecomunicat  
 NXP Semiconductors  
 Sapec  
 ST-Ericsson  
 STMicroelectronics  
 Synopsys  
 Technical Uni Delft  
 Technical Uni Eindhoven  
 Tedesys Global  
 Universitat Autònoma de Barcelona  
 Uni Cantabria  
 Vista Silicon

### Project leader:

Philippe Garcin  
 STMicroelectronics

### Key project dates:

Start: January 2010  
 End: April 2013

### Countries involved:

France  
 The Netherlands  
 Spain

Current hard-wired system-on-chip architectures suffer from a lack of flexibility which has a limiting effect on marketing potential. The primary constraints are excessive design cycle times and relatively high costs. In addition, process variability is not yet well addressed for 32 nm nodes and smaller. The objective of the CATRENE COBRA project is to develop and experiment with an open, flexible, high performance platform, substituting heterogeneous hardware/software subsystems with a regular array of processors. The COBRA platform will be driven by telecommunications, video and multimedia benchmark applications and will be demonstrated on 32 nm silicon with three-dimensional stacking.

Massively parallel processor arrays are now being used in high-performance embedded systems and for hardware acceleration in desktop computer and server applications, such as video compression, image processing, medical imaging, network processing, software-defined radio and other compute-intensive streaming media applications, which otherwise would use FPGA, DSP and/or ASIC chips.

At least 80% of new compiler technology users are expected to be many-core based within the next two years. The market is moving fast towards massive parallel architectures. It is also crucial for participating software companies to be in front of the technical innovation state of the art. However, design cycle times for hardwired system-on-chip (SoC) subsystems are close to two years, which is excessively long and costly.

### Cutting design time and cost

The main objective of the CATRENE CA104 COBRA project is to reduce the time and cost of the SoC design phase. This will provide European manufacturers with a strategic advantage in progressing new products from concept to production.

For this purpose, COBRA will develop an application-specific processor array. This massively parallel computing fabric will improve manufacturing potential and increase the energy efficiency of new SoC devices as a result of design uniformity. At the same time, flexibility will be maximised by encour-

aging development of software product derivatives. These will reduce development and manufacturing costs, as well as time-to-market, by comparison with hardwired alternatives.

COBRA will define, design and assemble the hardware computing elements as an interconnection of customisable processor clusters with embedded memory. These will be connected through a network-on-chip (NoC) device and be linked to the SoC host subsystem including three-dimensional (3D) graphics rendering support hardware, data and instruction caches, interfaces to cameras and liquid crystal displays.

The project will employ standard interfaces such as secure digital input/output, multimedia card and universal serial bus. The result will be a large 3D processing array hardware accelerator in 32 nm CMOS technology that combines flexibility and performance.

### Simplifying programming

Ease of programming is crucial for the development of the processing array. COBRA will offer a software environment which allows firmware developers to master the inherent complexity of parallel programming. A tool kit will allow generating, debugging and mapping tasks to be carried out on available computing resources.

COBRA will then perform the physical integration of



the computing fabric within the SoC hardware, taking advantage of 3D stacking. This will be followed by software integration within the host multimedia stack. System requirements will include energy and reliability management.

Finally, new techniques for parallel computing will be implemented in different application classes including those that are data-stream dominated as well as data/control hybrids. The main targets will include image post-processing chain and video codecs as well as multimedia in general, infotainment and communications.

### Multi-core platform

The project will benefit from co-operation between platform developers and platform users. COBRA will allow for the creation of an open multi-core platform to be shared with the European R&D community.

Key differentiators will include:

- Tool-assisted customisation of processors;
- A unique combination of advanced 32 nm process technology and architecture expertise derived from experience with applications;
- Dynamic management of process variability, fault tolerance and application quality of service;
- A real SoC output, with significant processing power, as part of a product roadmap;
- Advanced mapping tools to ease porting of algorithms to the platform, according to multiple programming models;
- Higher manufacturing yield at a given time with a shorter learning curve; and
- Aggressive metrics in terms of decreased time-to-market and power consumption, increased yield and scalability.

### Viable industrial path

This CATRENE project will secure the competitive power of European industry sectors such as telecommunications, TV, multimedia and high-performance computing. More generally, COBRA addresses any datastream application and provides an industrial path to make programmable accelerators viable.

The consortium involves three major European chipmakers and their partners. One member provides chips for a wide spectrum of digital consumer applications, with particular focus on set-top boxes, DVD players, digital TVs, radios, cameras and MP3 players. COBRA can considerably reduce time-to-market in these fields since it will provide a new methodology for rapidly assembling various product classes at different cost levels. Other fields include mobile phones, smart phones and the automotive industry.

COBRA will use Khronos standards, including OpenMAX, a royalty-free, cross-platform set of C-language programming interfaces. OpenMAX is intended for devices that process large amounts of multimedia data. One member of the consortium is an active member of the Khronos standardisation group, so the consortium anticipates the opportunity to disseminate results directly into the standard.

### Global competitive benefits

The CATRENE project will contribute significantly to the potential of its partners to compete in worldwide markets and, therefore, to extend employment opportunities. Consequently, this project will safeguard high-qualification jobs in the European nanoelectronics industry – including research centres involved in this field – and generate new jobs in small and medium-sized enterprises (SMEs).

It is expected that these jobs will be inherently more sustainable in the face of Chinese and other Asian competition due to the advanced technology and intellectual property underpinning the products developed from COBRA technologies.

COBRA will also significantly increase the degree of innovation present in future products from its industrial partners. The product portfolios of these companies will increase both in size and attractiveness on the market. This will help to preserve and create jobs at the contributing sites of several consortium members.

Finally, the project will create opportunities for SMEs by providing access to the high-technology results of larger companies. It is also expected that COBRA will help underpin the next generation of internal product development for participating SMEs.



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**CATRENE** ( $\Sigma!$  4140), the EUREKA Cluster for Application and Technology Research in Europe on NanoElectronics, will bring about technological leadership for a competitive European information and communications technology industry.

**CATRENE** focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

