Project profile

Cluster for Application and Technology Research in Europe on NanoElectronics

CT210 | High DYNAMIC range multi-processor for Ultra Low Power mobile devices [DYNAMIC-ULP]

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	✔
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	
More than Moore	
More Moore	✔
Technology nodes	28nm, 14nm

Mobile wireless devices are demanding even faster computing and transfer rates, as well as an increasing energy autonomy. To face these two constraints in a flexible way, DYNAMIC-ULP will propose to designers a technology leap forward: Fully Depleted Silicon on Insulator (FDSOI) CMOS. The project will define, build and validate advanced process modules and design platforms for 28nm and 14nm FDSOI on 300mm wafers. These two platforms will provide unrivalled foundations to address the exploding market of smartphones, tablets and communicating objects.

Partners:
ST-Ericsson
STMicroelectronics
SOITEC
CEA-LETI
ACREO
Infiniscale
DOLPHIN
Atrenta-France
Ericsson Mikroelektronik Ar-Ge Merkezi A.S.

Project leader:
Philippe Garcin
STMicroelectronics

Key project dates:
Start: 01 January 2012
End: 31 December 2014

Countries involved:
France
Sweden
Turkey

An expected flood of communicating devices

Tracing the development of the Telecoms market several decades backward, we see an inflexion point in early 2000, when location-to-location telephony moved to mobile telephony (people to people communications) and from 0.5 billion places to 5 billion people. Today, mobile phones are considered "internet-access in the pocket" devices. By 2025, it is predicted that some 50 billion everyday appliances will be "communicating" wirelessly with other devices through the internet ("internet of things"). And with the mobile society appetite for increasing amounts of multimedia content and additional functionality, and an expected flood of communicating devices, what we need are faster 4G mobile networks capable of handling LTE-advanced transfer rates (over 100 Mbit/s).

Permanent tuning possible at running time

To deal with these demands, DYNAMIC-ULP is to develop and validate advanced process modules and two design platforms (design kits, models and libraries) to ensure first silicon success of FDSOI CMOS 28nm and 14nm technologies on 300mm. A key advantage of FDSOI is to be permanently tuneable at running time to meet an optimal trade-off between performance and consumption. Hence these technologies will cover a wide dynamic range from 1.1v (to enable processors to run at 3.25 GHz) down to 0.4v (for long multimedia playback). With the expected ubiquity of communicating devices, a 10-fold reduction in power consumption is also a project objective. This reduction will be obtained by combining the FDSOI technology with a panel of innovative design techniques. The project will also target design enhancement, e.g. to help designers evaluating and optimizing power consumption as early as possible within the design flow.

Final demonstrators will be a high-complexity System on Chip (SoC) representative of 28nm FDSOI design rules; and a medium-complexity SoC representative of 14nm FDSOI design rules. But before scientific ideas reach their manufacturing phase, they need to go through two preceding phases: technological research and product development. Managed by STMicroelectronics, the project team comprises a consortium of ten European companies and institutions from the semiconductor industry and academia that can provide the necessary expertise for the first two phases, as well as technological facilities and pilot lines. Participating companies interestingly cover and stimulate value chains in a complementary way,

both at hardware level (Wafers, Silicon Circuits, Systems) and software level (CAD tools, Design Kits and Libraries, Systems on Chip).

A post-bulk vision

Studies of major players are converging on the fact that bulk processes are reaching their limit while looking for more performance in MIPS. The mobile processor giga-hertz race is forcing processors to use as high a voltage as possible at the expense of higher power dissipation. This requirement is no longer affordable for mobile devices, necessitating a high dynamic voltage range in order to address various deployment requirements. The chip will spend a lot of time in stand-by mode where the minimum leakage is mandatory, along with low-power, long-play-back multimedia accelerators, where the chip spends most of its time in standby mode. FDSOI technology is an answer, with the additional advantage that design porting from bulk will be both simple and fast.

Another innovation will be in design and architecture. Enabling such a wide dynamic range allows System on Chip architects a great measure of flexibility of choosing between keeping general host processors which need to be big, fast and power hungry, and dedicated hardware accelerators which can be used for specific tasks. The ability to run big processors fast, and the choice and availability of smaller power-efficient accelerators enable changes, not just at function level, but also at the System on Chip level where multiple functions cooperate. Several architectural innovations, based on product and market requirements, along with the ability to fully utilise such a large voltage dynamic range, are expected to evolve from this project.

A European synergy stimulating the whole value chain

DYNAMIC-ULP can generate business and technical benefits for European companies. After 15 years of constant growth, the mobile wireless market is now mainly fuelled by the replacement of outdated devices with smartphones and tablets. This has created a new segment with double-digit growth. This project supports the European effort to gain a leading position in electronic industry by enabling design and production of 28nm and 14nm CMOS technologies in Europe.

The strategic nature of the semiconductor industry has been recognized around the world, and this recognition has led to the continuous emergence of new geographic regions as future semiconductors hubs, acting as a powerful engine for economic growth and high quality jobs. In addition, the research intensity in semiconductor is proportionally higher than in any other industry and provides an adequate incentive to reinforce the presence of upstream industries, such as semiconductor equipment manufacturers and material providers. The association of R&D activities with volume production and strong manufacturing facilities also has a profound impact in developing local ecosystems.

The IC industry has been one of the fastest growing industries over the past 30 years, primarily because it has been able to offer a continuously decreasing cost per function to the electronics industry. This rise in economic value is the main reason, explaining the success and proliferation of integrated circuits in our daily lives. For manufacturing, improving and developing tools and methods to effectively manage this highly complex mix of technologies, processes and products – something DYNAMIC-ULP will contribute to achieve – will play a critical role in ensuring the future viability of the manufacturing facilities of our industry in Europe.

We cannot keep innovating without a powerful manufacturing base installed in Europe, making it necessary to maintain advanced prototyping activities in Europe, since it is the basis of future production runs and it may well help relocate production activities in Europe. DYNAMIC-ULP's design platforms in FDSOI 28nm and 14nm technologies will help achieve this, by joining with system architects, chip designers, CAD vendors and manufacturers.

Finally, there are clear benefits from having the ability to remain competitive and at the leading edge of technology for job creation and retention in the European Union. The project involves multiple countries within Europe and enables further employment opportunities in the future due to the new innovations being advanced in the project, especially enabling a continuation of advanced manufacturing, and a more fertile market for SOI wafers.

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

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