Cluster for Application and Technology Research in Europe on NanoElectronics

PROJECT PROFILE

CA703

Open ESL technologies to improve ESD productivity and quality
[OpenES]

By joining forces to provide missing links in system-level design, and to develop common, open and extensible solutions, the OpenES project will improve European electronics system design productivity and quality, as well as, Europe's competitive edge in this field. Based on an open electronic design and verification technology, these solutions will also provide an appropriate design framework and interfaces built on standards wherever possible, to significantly improve co-operation between IC/IP-provider and system integrator.

Integrating advanced complex systems is one of Europe's major strengths. However, its system-level design capability and ability to develop common, open and extensible solutions are suffering as the number of extra-functional properties (like timing, power and thermal information) and their importance increase. Crucially, a further demand for more features and improved functionality will make future systems dramatically more complex. Without advanced methods and tools to tackle these issues, the competiveness of European semiconductor companies and design houses is significantly hampered.

A standards-based solution can be found in electronic system-level design and verification (also referred to as ESL), an emerging electronic design methodology that uses appropriate abstractions in order to increase comprehension about a system, and also increase its chances of a successful and cost-effective implementation.

Common, open and extensible

The OpenES project will meet its objectives to improve system-level design and develop common, open solutions by:

1. Filling gaps in design flows with new interoperable tools and/or improving existing tools/flows;
2. Focusing on integral support of both functional and extra-functional requirements from specification to verification;
3. Improving reuse capabilities and supporting reuse of pre-integrated and pre-verified subsystems;
4. Enhancing interoperability of models and tools by upgrading and extending existing recent open standards.

The common open and extensible solutions, developed in the project and based on ESL, will provide an appropriate design framework and interfaces built on standards wherever possible. Extensions on standards will be initiated where necessary.

Key project deliverables will be:

- An industrial 'system toolkit' that describes and simulates the system-level design which traces various functional and extra-functional system properties, including the use cases;
- Code generators to obtain the architectural view including both software and hardware from the system model;
- Extensions to current standards to integrate (existing) IPs and subsystems representation at system and architectural levels. Both digital and analog/RF IPs are considered;
- Cross abstraction-level and multi-property verification methodology to verify and validate the system properties of use cases defined during system specification;
- Definition of interfaces to support domain specific simulators and back-annotation of extra-functional properties;
- Validation of system-design flow and associated tools and methods using real industrial cases and proof-of-concept demonstrators (PCDs);
- Training courses to familiarise participants with system-level issues and solutions.

PROJECT CONTRIBUTES TO

- Communication
- Design technology

PARTNERS

CISC Semiconductor GmbH
DOCEA Power
ECSI
Magillem Design Services
STMicroelectronics
Thales Communication & Security
Thales Research & Technology
NXP Semiconductors N.V.
Synopsys
Vector Fabrics
Evatronix Spolka Akcyjna
Indra Sistemas
CEA LIST
UJF-VERIMAG
Technische Universiteit Eindhoven (TUE)
Universitat Autònoma de Barcelona
University of Cantabria

COUNTRIES INVOLVED

- Austria
- The Netherlands
- France
- Poland
- Spain

PROJECT LEADER

Laurent Maillet-Contoz
STMicroelectronics

KEY PROJECT DATES

April 01, 2013 - August 31, 2016

European effort reaps benefits

The OpenES consortium presents a balanced research effort between industrial partners, public research institutes and higher education universities. Academic partners and research centres are also involved to provide theoretical background and advanced techniques to address the technical challenges to be tackled by the project.

OpenES project is supporting the European effort towards strengthening the global position of the European design houses, semiconductor industry, EDA vendors and IP and subsystem suppliers by improving the system-design quality and productivity. This project also contributes to maintaining state-of-the-art technology at the universities and research institutes, ensuring high education standards for undergraduates and doctorate candidates in the future.

OpenES will impact European industry in two ways. Firstly, it will enhance the system-level design to reduce development costs by improving the co-operation between the system houses and the semiconductor companies, and by establishing an ecosystem based on open standards to create high-level models and associated tools, thus avoiding the expensive development of in-house proprietary approaches and tools.

Secondly, OpenES will optimise products to increase competiveness by innovating product architectures and increasing efficiency in product design with less redesigns, reduced system development cost and faster time-to-market. Furthermore, it will increase Europe's to design heterogeneous and embedded systems in a more optimised and systematic manner. Together, it will maintain Europe's leading position in product innovation and design in major applications.

Promising markets

The EDA market grew 9% in 2010 and 14% in 2011, reaching US$4.19 billion worldwide in license and maintenance revenue last year (excluding services and IP). The sector employed more than 26,000 people at the start of 2012. A steady 10% growth rate is predicted for the next five years, sustained by a continuous shift of design methodology to the ESL level. The increasing role of ESL in overall IC design flow is indeed expected to foster the market for new dedicated EDA tools.

Regarding the IP and subsystems market, development costs of a single system-on-chip (SoC) is over US$ 85m and this cost is rising rapidly. The industry has reacted to these rising costs through the concept of IP blocks: functional components that act as building blocks which can be integrated into a SoC. The SoC market is expected to grow from $85.9 billion in 2011 to $117.8 billion in 2016, at a CAGR of 6.47% from 2011 to 2016.

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CATRENE (E! 4140), the EUREKA Cluster for Application and Technology Research in Europe on NanoElectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.