PROJECT PROFILE

CAT 601

Holistic design methodology improves system integration resulting in shorter time-to-market, lower costs, higher design reliability and better performance

[SiPoB-3D]

While compact system-integration is crucial, this process is also expensive and the risk of failure high due to complexities. This is why a good design environment with a simulation facility is needed to allow designs to be simulated and undergo extensive pre-fabrication testing and changes – but without the normal costs – before they are finally released for manufacturing. This is the sort of design methodology the Co-Design for System-in-Package-on-Board (SiPoB-3D) project aims to deliver.

For compact system-integration, technologies, like More Moore (MM), More than Moore (MtM), three-dimensional high-density 3D IC, system-in-package (SiP), as well as passive integration, are combined. This process also involves other technologies and a variety of different materials. For example, a complex SiP set-up could include such advanced technologies as through silicon via (TSV), through encapsulant via (TEV), redistribution layers (RDL) and micro-bumps. Importantly, with the risk of failing too high for such complex SiPs, expensive prototypes cannot be fabricated without a proper design and simulation environment for extensive pre-manufacturing simulations (like design-rule checks, and thermal and electrical interactions). A coherent chip-package-board co-design environment is therefore called for.

Holistic approach means faster, better and more economical

The SiPoB-3D project aims to investigate and develop an efficient, holistic design methodology that will focus on system optimisation, and which includes chip, package and board as a whole. A feature that makes this methodology efficient and attractive is the avoidance of expensive actual test-and-change design iterations, which is achieved through the use of simulation software. It is also important to have a methodology for mapping the best technology available to a manufacturer to design the optimum SiPoB-3D device faster, better and more economically. Using a holistic approach, SiPoB-3D's activities will include investigating and simulating models which enter into a design library; developing a design methodology; and studying the setting-up an optimum system. Data transfer between the different domains, especially between the board suppliers and chip/package suppliers, needs to be optimised so that an optimal subsystem can also be achieved on board level.

In short, this methodology will deliver the following basic – but crucial – elements needed to create a coherent chip-package-board co-design environment:

- An optimised SiP which best fits a customer board and with an optimum layout;
- Faster and fewer design cycles (thanks to simulation);
- Lower costs (thanks to simulation);
- Higher reliability;
- An optimal interface between the three different domains;
- Optimal data transfer between participating companies;
- The best performance;
- And the shortest time-to-market.

The SiPoB-3D project will not only deal with the design of a compact system. It will also provide test-tools for hardware, modelling and methodology assessment. These tools will include advanced chip technologies, and novel chip-embedding and die-stacking technologies. Digital and analogue logic, as well as mm-wave design, will be investigated, and possible standardisation considered. The physics of different building blocks that go to produce a SiPoB-3D will also be explored and implemented. In addition, material parameters will be investigated. These are of crucial importance for a proper design environment (for high-frequency analogue designs, for example).

On a board level, system designers will investigate profitability and other economic aspects of newly explored modules. Reduced development time and cost-reduction are expected, thanks to additional modularity. And the new SiPoB-3D tools will also ensure that data exchange (between chip, SiP/module and system) takes place at an earlier stage in system development.

PROJECT CONTRIBUTES TO

Automotive and transport

Design technology

More than Moore

More Moore

PARTNERS

Infineon Technologies AG
Continental Automotive GmbH
Computer Simulation Technology GmbH
Hitex GmbH
Schoeller Electronics Systems GmbH
Symeo GmbH
STMicroelectronics SA
STMicroelectronics (Grenoble 2) SAS
Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e. V. (FhG)
with its institutes EAS/IIS and IZM ASSID
FAU Erlangen-Nuremberg
CEA-LETI
Université de Savoie IMEP- LAHC, Chambéry, Le Bourget du Lac

COUNTRIES INVOLVED

Germany
France

PROJECT LEADER

Klaus Pressel
Infineon Technologies AG

KEY PROJECT DATES

01 March 2016 - 28 February 2019

Experienced project consortium

The project consortium is well-balanced and provides needed in-house experience and expertise to cover all three domains – chip, package and board – as well as technology and advanced applications. This consortium comprises two leading European semiconductor chip suppliers with major packaging, R&D and production operations in Europe; a company that focuses on electromagnetic and multiphysics simulations and software for chip, package and printed circuit board; and suppliers of printed circuit boards, tools, software components and prototypes for electronic systems. In addition, four research institutes, which specialise in such areas as design, 3D and high frequency, are also project participants, as are two companies with world-leading experience in automotive and mm-wave applications.

Enriching European supply-chains

SiPoB-3D will strengthen the European electronics and related industries in several ways. Chip producers will improve their system integration capabilities; computer simulation and design companies will be able to enhance their tools; and electronic design automation (EDA) and board suppliers will learn to better link their technologies to semiconductor suppliers and provide the basis for setting up mini systems (modules or mini boards).

In addition, application-driven companies can push their applications towards faster system-integration. SiPoB-3D will also ensure that the design process is faster and more efficient, thus reducing time-to-market and increasing system reliability. Furthermore, the close cooperation of design-tool, semiconductor, board and application-driven (automotive and high-frequency) manufacturers will further improve time-to-market, reduce development effort and optimise system costs. This will, in turn, also drive new competitive products through the European supply chain, and secure competitive power in all European industry sectors where SiP integration is applicable.

Crucial developments and markets

Of course, it is also crucial to the future of this project that there is sufficient market demand for the products it is helping to design, develop and manufacture through its methodology and supporting tools. Although SiP is currently driven by smartphones, tablets, and gaming devices, there is increasing demand in all key sectors, including automotive, where industrial products are found, as well as Internet of Things (IoT). According to a MarketsandMarkets report, the SiP market is likely to witness high growth in the coming years due to growing markets and the increasing need for advanced architectures in electronic products. The SiP market is expected to grow from US$ 5.44 billion in 2016, to US$ 9.07 billion by 2023, at a CAGR (compound annual growth rate) of 9.4% between 2017 and 2023.

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