CATRENE
Cluster for Application and Technology Research in Europe on NanoElectronics

PROJECT PROFILE

CAT801 | Ramping up high-volume TSV manufacturing and ensuring a better production yield [TSV-Handy]

In particular, TSV-Handy will deal with the handling of heterogeneous 300mm wafers with edge trim inspection, and the development of metrology and new logistical concepts for wafers on 380mm frames. It also aims at improving temporary bonding and debonding processes.

Through silicon via (TSV) is a so-called 'more-than-Moore' (MtM) technology that enables new chip architectures. As we move to the 10nm node, TSV will become a required technology for system design. Notably, TSV improves the density of a device by stacking dices (3D) onto an interposer, or arranging them horizontally side-by-side (2.5D). This technology is also applied to reconstituted epoxy/mould compound wafers with TPV in fan out wafer-level packaging (FO-WLP) technology, an enhancement of standard wafer-level packages developed to provide a solution for semiconductor devices requiring a higher integration level and a greater number of external contacts. It provides a smaller package footprint with higher input/output (I/O), along with improved thermal and electrical performance.

Project members contribute own in-house solutions

The first TSV products, like the Xilinx Heterogeneous 3D FPGA and the Micron Memory Cube, are already appearing on the market. Thus feasibility is not in question. However, in order to make the industrial and business model viable, it is necessary to support the ramp-up of high-volume manufacturing (HVM), and to optimise the yield along the value chain. That's where TSV-Handy' will play a key role in achieving this.

In particular, TSV-Handy will deal with:

- Handling of heterogeneous 300mm wafers with edge trim inspection;
- Developing metrology and new logistical concepts for wafers on 380mm frames;
- Improving temporary bonding and debonding processes.

Importantly, several consortium partners – notably RECIF, ENTEGRIS, EVG, FOGALE, and NANIUM, together with STMicroelectronics, CEA Léti and Imec – are already involved in some of these issues and will contribute significantly with products and expertise. In addition, results and deliverables from past and current CATRENE and ENIAC JU projects will also be used effectively.

A first project challenge is set by the multiplication of heterogeneous types of wafer on a 3D TSV line, which are presenting highly different mechanical behaviours and physical properties. RECIF targets the development of a 300 mm wafer-handling platform, which supports as many types of wafer as possible, without having to reconfigure the equipment or swap dedicated modules (like the end effector). This will help end-users benefit from equipment flexibility and 'up time', because the current solutions are still unstable. RECIF will cooperate with STMicroelectronics, NANIUM, CEA Léti, imec and FOGALE in defining the key substrates to be handled on the same platform in an industrial environment. Targets will also be defined to ensure the best balance between: equipment flexibility (number of wafer types addressed), stability (up time) and cost of ownership.

A second challenge involves the handling of ultra-thin wafers (around 50μ thickness), after they are 'debonded' on film frames. FOGALE is supplying metrology and inspection solutions for 3D IC TSV, 3D MEMS, 2.5D and advanced packaging applications. Its metrology technologies address TSV dimensions without aspect ratio limitation, temporary bonding and TSV wafer thinning.

For advanced packaging applications, such as the fan-out (FO) process, the tool developed by FOGALE will be used to measure moulding compound thickness, wafer flatness and silicon thickness. This tool will also perform metrology for wafer on frames, such as top thin layer, silicon and tape thicknesses and total thickness variation. For Taiko wafers, the FOGALE tool measures thickness, nm-level backside roughness and Taiko ring eccentricity. Furthermore, a fully automated metrology solution will be developed and installed at NANIUM for assessment and demonstration. In order to support the development of fully automated equipment, ENTEGRIS will work on the design and prototyping of new carriers (or cassettes) for the shipping and processing of wafers mounted on film frames.

CATRENE
Cluster for Application and Technology Research in Europe on NanoElectronics

PROJECT CONTRIBUTES TO

- Communication
- Design technology
- Process development
- Manufacturing science
- More than Moore

PARTNERS

RECIF
ENTEGRIS
EV Group
FOGALE
Nanotech
NANIUM
STMicroelectronics
Institute CEA Léti
Imec

COUNTRIES INVOLVED

- France
- Germany
- Austria
- Portugal
- Belgium

PROJECT LEADER

Guilhem Delpu
RECIF

KEY PROJECT DATES

1 April 2015 - 31 March 2018

The technical goal for the work on temporary bonding is to integrate the coating and bonding capability for 'novel adhesives solutions' inside an EVG bonder tool in order to increase the throughput and performance of the temporary bonding process using these new adhesives solutions. EVG will work on this process, as applied to NANIUM 300mm silicon and 300mm reconstituted wafers. And the technical goal for the work on debonding is to implement in the debonding tool. Temporary bonding and debonding tools address the 'mid-end', which require a higher degree of cleanliness as compared to classical packaging types of process tools.

Increase in demand for TSV products and production tools

The project will ensure productivity increase on the one hand, but also generate new products (thin packages, 3D system integration, package-on-package, for example), and therefore more business, which will raise employment. It will also promote and maintain high-tech European companies and semiconductor centres.

In particular, the production of TSV chips and wafers is forecast to have a significant average continuous growth rate in the coming years (107 % throughout 2013-2018), given that industry can address the challenges related to technology and manufacturing cost.

This project secures the competitiveness in several European industry sectors. The FO packaging market is just starting, as this new technology platform begins implementation. According to YOLE, a French research institute, today 90% of the FO-WLP market is determined by eWLB, a breakthrough technology which provides a more space-efficient package design, enabling a smaller footprint, and higher density input/output. In addition, the production of ultra-thin wafers is increasingly required in numerous applications, where ultra-thin wafer processing does not only include thinning and dicing issues; but also their handling. Since tapes can no longer be used for ultra-thin wafers, new wafer-handling technologies have to be developed, which means that the use of temporary bonding technology is growing. Along with standard approaches comes temporary bonding, with reconstituted wafer for FO-WLP.

By 2016, the temporary bonding tool market value for TSV and FO-WLP will be US$222m. The TSV Handy project will also help boost and stabilize this position for the novel applications targeted in the TSV Handy project. This is particularly important for Europe, as the major competition is in Asia and US.

Then there is metrology inspection. Here Europe offers more flexible and versatile solutions to its customers over the competition, as it is the only solution-provider to be able to measure moulding compound before thinning for advanced-packaging solutions. TSV Handy will help improve equipment to satisfy current and upcoming demands. Potential sales for a key European supplier are €2m-4m for 2015-2018, and €5m-10m for the next three years.

Regarding automated wafer-handling equipment, new business for a key European supplier is expected to drive up to 30% more volume. Estimated revenue generated from this segment would be in the range of at least €5m per year by 2020. In addition, for a key European automated shipping carrier supplier, who already has some 40% of the worldwide market, Europe represents 20% of this business. It is expected that the project deliverables will generate a 40-60% share worldwide, with 40% of that business in Europe. Finally, that same supplier also expects more than 60% market share in in-fab 3D wafer-handling product worldwide, with 30-40% of that business in Europe. And a 45% worldwide market-share, with 50% of it in Europe is expected.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

CATRENE (E! 4140), the EUREKA Cluster for Application and Technology Research in Europe on NanoElectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.