PROJECT PROFILE

2A703: Networks on chips design driven by video and distributed applications (NEVA)

EDA FOR SOC DESIGN AND DFM

Partners:

ACE
Bull
Certess
LETI / CEA
LIACS / Univ. of Leiden
Philips
Silicomp
STMicroelectronics
TIMA / INPG
VERIMAG / UJF

Project leader:

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Key project dates:

Start: January 2005
End: December 2008

Countries involved:

France
The Netherlands

Circuits for electronic devices are becoming so complex that they are expected to reach a billion transistors by the end of 2008. Traditional silicon chip architectures are nearing the limit of their performance in such applications so the NEVA project was set up to introduce innovative network-on-chip designs, based on multiple processors and asynchronous circuitry. The goal is to allow designers and application engineers to cope with emerging applications resulting from multimedia/communication convergence. In the first instance, datastream applications, mainly from the video environment, will be used as drivers, with a targeted computing power around one giga operations per second per chip.

Increasing awareness of bottlenecks in today's system-on-chip (SoC) designs motivated chipmakers Philips and STMicroelectronics, and computer systems company Bull, to propose a project devoted to network-on-chip (NoC) design. The aim is to provide designers and application engineers with an alternative approach to complex circuit architectures capable of handling giga operations per second (GOPS) for 130, 90 and future 65 nm technology generations. The MEDEA+ 2A703 NEVA project will be driven mainly by video system requirements, with complementary functions proposed by Philips in video processing and STMicroelectronics in video transmission. Over the next few years, video applications will have to handle increasing quantities of data for high-definition TV with demanding enhancements such as three-dimensional display from two-dimensional data extraction. Approaches proven in the design of video applications are expected to benefit other datastream applications.
NEVA will address inter-process communication at chip level, using communication-centric design techniques. Bull will provide the required applications technique for benchmarking in the field of multi-computing and high-performance computing (HPC).

Three innovative techniques

To reach its goals, NEVA aims to implement and prove three innovative techniques:

1. **Communication-centric design** using a high level approach based on system level mock-ups. Transaction-level modelling (TLM) is more and more accepted by industry. This approach will be extended while efficient protocols and fast co-verification methods, such as simulated and accelerated TLM, will be developed for NoC architectures. The benefit will be shorter time to market through accelerated simulations and reusable models at intermediary level.
2. **Dynamic configurability** will allow optimisation of resources. This aspect will be considered at architectural and modelling levels. New timing tools will be necessary to guarantee predictability. Compilers have to be adapted to take into account customised complex instructions that will reconfigure the hardware resources accordingly. This approach will result in higher comput-

ing power and suitability for demanding real-time applications.

3. **Asynchronous architectures** implemented using the globally asynchronous locally synchronous (GALS) technique. This will result in the ability to design circuits with lower power consumption. Clock distribution problems will be reduced as well as associated speed limitations. Yield will be increased as a result of the greater reliability of GALS systems.

Achievements from the first phase of MEDEA+ — including A302 ESPASS-IS, A502 MESA, A508 SPEAC and A511 TOOLIP — will also be exploited and are expected to provide a considerable advance.

Building on global success

In the domain of multi- and high performance computing, Bull is among the few European players capable of being competitive against US and Japanese counterparts. Although competition from China is strengthening, Philips is in the top three worldwide and number one in Europe for consumer audio/video electronics. STMicroelectronics and Philips provide chips for a wide range of digital consumer applications such as set-top boxes, DVD players, digital TVs, radios, cameras and MP3 players. STMicroelectronics is the world's leading supplier of MPEG video compression devices with over 140 million chips sold.

The electronic design automation (EDA) market is currently estimated at €3.2 billion and is expected to grow at a rate close to 5%. Quality evaluation of hardware blocks, computer-aided design (CAD) tools for protocol verification and the accelerated transaction-level platform are three sectors in which European CAD tool suppliers and NEVA partners Certess and Silicomp will gain substantial benefits — such as expertise, improved fit with industrial needs and new products. Tools will target new market segments the size of which is still difficult to estimate.

In global values, the world semiconductor market is expected to reach around €200 billion in 2005, and to slowly increase from this value in 2006 and 2007. Products addressed by NEVA concern data processing and fall in the category of application-specific standard products, which constitute roughly 25% of these amounts — i.e. around €50 billion.

Securing competitiveness

Overall, this MEDEA+ project is intended to secure European competitiveness in TV, telecommunications, multimedia, and multi- and high performance computing. NoC-based ICs will target the set-top box and camcorder markets. NEVA is also addressing datastream applications in general.

The global digital TV market is set to grow from 58 million units in 2003 to 91 million in 2008, an average growth of 8 to 9% but growth will only take off from 2006 as integrated digital TVs become mainstream. Availability of low cost set-top boxes could change the dynamics of the conversion to a digital TV service in Europe. Their price level is already expected to fall from €84 in 2003 to €36 by 2007. Production of mobile cell phones is expected to stabilise at around 520 million units a year from 2005. Video compression and video enhancements will hopefully contribute to revitalising their sales. Electronic games are also very demanding in terms of video-computing resources. Finally, distributed applications will increase their performance and attractiveness thanks to the different network levels promoted by this project. The current camcorder market is around €1.1 billion, and growing at 10% a year.

Reinforcing position

Europe has a strong scientific advance in system-level design techniques compared with the rest of the world. Background and synergy from NEVA partners will help Europe to keep and reinforce this strong position. New approaches developed in the project — such as asynchronous design — will be disseminated effectively within the European designers' community.

The NEVA project is also expected to favour the creation of new jobs in the participating CAD companies. The advantage in terms of competitiveness for the participating chip making and system companies will be a positive influence on employment in France and the Netherlands with the potential to create additional employment in peripheral businesses around Europe.

With three university laboratories and one public research centre participating in the project, a substantial impact on education is also expected. Innovations resulting from the project, at theoretical and methodological levels, will influence existing courses and give birth to new courses. Bull intends to strengthen its co-operation through lectures on system prototyping at the ISEP engineering school by extending courses with the validation of protocols.

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.