PROJECT PROFILE

2A708: Low power expertise for mobile and multimedia system applications (LoMoSA+)

EDA FOR SOC DESIGN AND DFM

Partners:

CEA
DS2
Philips
STMicroelectronics
Thales
Thomson
TIMA Laboratory
Uni Lugano (AlaRI)

Project leader:

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Key project dates:

Start: January 2005
End: December 2008

Countries involved:

France
The Netherlands
Spain
Switzerland

The increasing amount of heat dissipated within portable electronic devices is a growing concern for consumers and manufacturers alike. The MEDEA+ LoMoSA+ project aims at the creation of European low-power expertise in this domain. This project will enable fast development of future battery-operated devices that combine high computing power with ultra low power dissipation and low cost for new applications such as portable personal video receivers, 4G phones and mobile TV. For mains-operated devices, the project results will help to avoid expensive packaging and forced-air cooling. Many of the low-power optimised LoMoSA+ deliverables can also be used in future application-specific projects.

An extrapolation from today's high performance deep-submicron electronic devices implies the need for packing ever-increasing amounts of power into very small volumes. Consequently, if left unchanged over the next decade, system temperatures would rise from the equivalent of a warm dinner plate to that of the surface of the sun.

Design of systems and complex integrated circuits (ICs) in future deep submicron technologies — 65 nm and below — requires hugely innovative solutions to control dynamic and static power consumption, and to reduce exponentially increasing power leakage.

Previous designs involved tradeoffs between delay, throughput and volume; new complex designs must now balance delay, throughput and power consumption. Low-power design is the enabling technology and a critical prerequisite for the technical and commercial success of many future applications, including those in mobile telecommunications.

Overcoming significant constraint

Many MEDEA+ projects are concerned with application domains where low power is a significant design constraint. The MEDEA+ 2A708 LoMoSA+ project focuses on building European expertise in low power. It will provide a major boost in efforts to reduce overall power consumption — active and stand-by — in systems by more than 70% as early as 2008.

However, there is no 'silver bullet' solution. Improvement in overall power consumption has to be achieved through reductions at all levels of systems development: architecture, software, circuit design, libraries and devices. Therefore, LoMoSA+ is taking a holistic approach for power-aware systems.

The project investigates low-power solutions that can be implemented in current bus-controlled system-on-chip (SoC) devices. It also covers the impact on power, scalability and performance of future multiprocessor SoC infrastructures, based on novel on-chip communication solutions.

These next generation SoC architectures communicate through a distributed network-on-chip (NoC) architecture, which will have higher power needs. To meet such complex demands and reduce the design cycle, LoMoSA+ aims to develop further the concept of hardware-dependent software (HdS). This depends directly on the underlying

hardware. It enables real concurrent development and low-power optimisation of both hardware and software in SoC design, helping keep power consumption under control.

Project partners include world-class experts from all MEDEA+ partner groups, including chipmakers and systems manufacturers, as well as a number of university research laboratories and a fabless silicon design house.

Developing low-power platform

LoMoSA+ will achieve its goal by initiating development of a European low-power platform for mobile and multimedia applications. This will consist of an interactive combination of architectural models, design flows and methodologies, hardware design components, embedded software and test benches.

Key deliverables correspond to platform components and include:

- Architectural templates for mobile low-power multimedia applications;
- Low-power optimised hardware intellectual property (IP) blocks and libraries;
- HdS-based design tools for multi-processor SoCs; and
- Low-power design tools.

Interaction between these deliverables will be demonstrated for some specific mobile multimedia applications.

Project consists of five packages:

1. Identification and specification of architectural templates for advanced multimedia and low-power applications — the challenge is to define an architectural template suitable for a variety of standards and future applications;
2. Design of advanced low-power IC modules and components — this covers design of functional IP blocks for the low-power platform, and includes investigation of low-power library blocks and on-chip communication. The recent great success of microelectronics is mainly due to geometric scaling, reducing the cost per gate for every new technology node — Moore's law. But extra functionality per chip and increased performance requirements have doubled power consumption of processor chips every three years. The challenge is to design IC modules and components that will keep this exploding power consumption under control.
3. HdS and real-time operating system (RTOS) inside a multiprocessor SoC — low clock rates in conjunction with lower voltages are one of the most valuable contributions to power saving in programmable devices and this can be achieved by using multiple processors with lower clock rates instead of one processor with a high clock rate. In practice, programming these parallel architectures is a challenge, while tool support is almost non-existent. Using a distributed NoC architecture will have some intrinsic power saving thanks to the wiring reduction — and NoC provides the basic on-chip infrastructure for smart power management that will maximise power efficiency by implementing voltage and frequency scaling and/or power-down features. Accordingly, the HdS layer needs to be adapted to these new requirements.
4. Development of new design methods and tools for power modelling, exploration, optimisation and verification during all phases of SoC design — this involves exploring design methods and tools at different levels of the design hierarchy: system, architecture and logic/circuit. Challenges include high-level power estimation and optimisation, tools for application profiling, best partitioning and optimised mapping, and power simulation and optimisation for complex analogue/mixed signal blocks.
5. Definition and development of low-power mobile multimedia demonstrators — these are the proof of the pudding for hardware, software and HdS components developed in the other work packages.

The horizontal structure of LoMoSA+ places it in an ideal position to exploit best solutions. Many of the low-power components developed, as well as the techniques and methods, could also find their way into other advanced technologies.

Critical for digital society

Development of low-power design expertise is critical for future European technical and commercial success in many application areas, particularly mobile telecommunications and multimedia. Whoever solves the power consumption problems in a comprehensive and systematic way will be the clear winner globally, leaving little room for the competition.

Therefore, the low-power technologies and methodologies being developed in LoMoSA+ will place Europe in a leading position for the associated market segments. The expertise-oriented approach initiated in this MEDEA+ project is a major step forward to arrive at a general European low-power platform.

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.