MEDEA+

PROJECT PROFILE

2T101: Strained silicon-on-insulator substrates for high performance ICs (SilOnIS)

IC TECHNOLOGY INTEGRATION

Partners:

Accent
Aixtron
AMD Saxony
ASM
CEA-LETI
Freescale
Infineon Technologies
Jobin Yvon
OMI
Philips
Siltronic
SOITEC
Sopra
STMicroelectronics

Project leader:

Bruno Ghyselen,
SOITEC

Key project dates:

Start: January 2005
End: December 2007

Countries involved:

France
Germany
Ireland
The Netherlands
United Kingdom

Two novel breakthrough technologies — high mobility strained silicon and silicon on insulator (SOI) — are being merged on the same materials platform to create a new European industrial source of large diameter wafer substrates for the fabrication of integrated circuits (ICs). This platform will be used initially for sub-65 nm CMOS nodes employed primarily in high performance chips. The MEDEA+ SilOnIS project combines the strengths of the leading European manufacturers in the fields of substrate materials, metrology and devices to develop jointly the fabrication technology for strained SOI wafers. The resulting wafers should be available commercially soon after the end of the project.

As devices become ever smaller, there is need to enhance performance without paying dramatically increasing costs for feature size reduction. New materials and substrates are being developed to overcome technical limitations of conventional silicon wafers.

The MEDEA+ 2T101 SilOnIS project aims to build a technology platform for strained SOI wafers, bringing together the main European players in substrates, chipmaking and metrology to secure development of high mobility SOI wafers and to demonstrate and speed use in chip fabrication.

SilOnIS will combine high mobility wafer-level strained silicon and SOI in a single technology platform for high performance chips. This new generation of smart substrates offers a radical approach in that the strain created is kept constant during the subsequent process flow. Thus the substrate platform delivers the processing compatibility of these new substrates with sub-65 nm technology in industrial chipmaking.

Meeting industry needs

The International Technology Roadmap for Semiconductors (ITRS) recommends a mobility improvement to fulfil drive current specifications. This enhancement must be significant for the high performance 45 nm node and more limited but still marked for the low power 45 nm node. For sub-45 nm nodes, the requirement is even higher. This can be achieved using strained material, for which an improvement of 80 to 100% can be achieved in long channel mobility.

Use of SOI technology is the most valuable way to improve performance. Lower parasitic capacitance, better sub-threshold swing for fully-depleted devices, and floating body effect for partially-depleted devices are the most significant SOI-related aspects that increase speed and reduce power consumption. A combination of strained and SOI materials is one of the most interesting ways of enhancing circuit performance.

A well-known approach to strained silicon is 'local' or 'process-induced' strain, based on the uniaxial strain introduced during CMOS manufacture. It is very successful and leading edge chipmakers have implemented it in 90 nm technology manufacture, in bulk and in SOI technologies.

Global strain defined by a biaxial strained silicon layer at the substrate level can boost

device mobility and current drive. It helps overcome the limitations of uniaxial techniques and, combined with local strain techniques, maximises performance for future technology nodes. It is independent of a specific MOSFET geometry, and applies to large and submicron devices. Global strain is not only an alternative but can be combined with process-induced strain to enable optimisation of NMOS and PMOS transistors.

The nodes addressed are later 65 nm generations but the focus is on 45 nm. The intention is to establish a common platform related to strained SOI technology, starting with appropriate substrates, suitably adapted to the sub-65 nm fabrication flow. Each end-user will be able to adapt the results to its own needs and roadmap.

Reliable and mature fabrication

SilOnIS proposes a complete innovative solution to meet challenges raised by the ITRS. Specific objectives involve materials, devices, metrology and characterisation.

The first objective focuses on materials. The aim is to provide an industrial source of large diameter strained SOI substrates by developing a reliable and mature fabrication route for high mobility SOI wafers. It also anticipates the advanced substrate requirements of chipmakers for volume quantities.

Key parameters are quality – in terms of defect rates, uniformity of thickness, strain control, etc. – and volume compatibility. Cost is also a vital factor as it impacts directly the market share that such a technology can address. Naturally, 300 mm wafers are the final target and will quickly become the standard diameter within this project – early phase and advanced R&D experiments will consider 200 mm wafers.

The project will also authorise strategic access to early and rare prototypes of these material developments to enable European end-users involved to initiate their own R&D into these new strategic materials as early as possible.

Development of key intellectual property (IP) from early R&D is also an objective. Prototype materials will have to meet a certain number of specifications that allow them to be introduced into advanced manufacturing.

There will be a sharing of costs and expertise relative to the technological steps involved in wafer manufacture – such as silicon/silicon-germanium (SiGe) cleaning, thermal treatment and oxidation, etching, strained silicon epitaxy and oxide (TEOS) deposition. Such collaboration will reinforce and safeguard European leadership in materials, especially in substrate manufacture where SOITEC and Siltronic are world leaders.

A key element is that the materials targeted are high-end substrates combining innovation with high added value. European equipment suppliers will be strengthened, especially in the field of metrology and characterisation in strained silicon and SOI as well as in manufacturing processes, such as SiGe/strained silicon epitaxy.

Device demonstrators

The second specific objective is related to devices. To validate and guide materials developments at device level and to shorten introduction of next generation substrates in chip fabs, the project aims to produce a demonstrator integrating high mobility SOI wafers with sub-65 nm technology. This will ensure a good position for future device and circuit developments.

Device demonstrators combining high mobility materials and SOI architectures will be produced as early as possible.

SilOnIS will collect a maximum amount of technical information at the substrate integration level based on combining high mobility materials and SOI architectures at the substrate level to assess better this 'global' strain approach compared with reference 'local' or 'process-induced' strain approaches.

Sharing of costs and efforts to assess the present approach will be a key feature. It will also be necessary to acquire strategic IP related to this new platform and stay well-positioned compared with aggressive players in the USA and Asia.

Specific metrology

In the third specific objective, SilOnIS is oriented to specific metrology focusing on strain, germanium content, defect rates – such as threading dislocations and pile-ups – and other parameters arising from introduction of high mobility SOI wafers into CMOS manufacturing.

This third building block aims to ensure material suppliers and end-users at the device level will find adequate metrology and characterisation tools to assess the quality of SOI wafers for technology development in the short term and volume manufacture in the longer term. It also aims to develop relationships with an assembly of European equipment suppliers in this specific area.

MEDEA+ Office
140bis, Rue de Rennes
F-75006 Paris
France
Tel.: +33 1 40 64 45 60
Fax: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

MEDEA+ Σ!2365 is the industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.