PROJECT PROFILE

2T103: Integration of 45 nm CMOS technology (FOREMOST)

TECHNOLOGY PLATFORM FOR NEXT-GENERATION CORE CMOS PROCESS

Partners:

Air Liquide
Aixtron
ASMI
Carl Zeiss
CEA-LETI
CNR-INFM-MDM
CNT
Epichem
Freescale
IBS
IMEC
IMS-CHIPS
INPG-IMEP
Jordan Valley
LAHC Uni Savoie
LMGP/CNRS-INPG
LTM-UJF
NCSR Demokritos
Philips
Qimonda (former Infineon Technologies)
STMicroelectronics
Vistec Semiconductor (former Leica Microsystems Semiconductor)

Project leader:

Danielle Thomas
STMicroelectronics

Key project dates:

Start: January 2006
End: June 2008

Countries involved:

Belgium
France
Germany
Greece
Israel
Italy
The Netherlands
United Kingdom

To maintain Europe's lead in CMOS integrated circuit manufacture, the FOREMOST project is developing and demonstrating advanced process modules and transistor architectures for a full 45 nm node technology in industrial 300 mm wafer fabrication plants. The project targets both CMOS logic and DRAM/FLASH memory process technologies, and is promoting synergy between the competences of leading European semiconductor manufacturers. The objective is to enable key players to be able to propose the most advanced logic technologies ahead of the globally predicated road map – safeguarding and boosting the position of Europe's chipmakers and their equipment and materials suppliers in the world market.

Much of the success for modern electronic systems comes from the continual reduction in size combined with dramatic increases in performance of the basic semiconductor chips. Worldwide co-operation has resulted in the International Technology Roadmap for Semiconductors (ITRS) which indicates global consensus on timing for successive generations of CMOS technologies – often expressed in terms of circuit feature or 'node' size – to maintain this progress.

All the major manufacturers of CMOS logic and DRAM memory chips have mass production at 90 nm node technologies. MEDEA+ projects are ensuring that 65 nm node technologies are in an advanced state of industrial development and expected to enter in full production in 2007 at the latest. And 45 nm node technology modules are now being actively investigated by the major chipmakers for industrial production in 2010.

The MEDEA+ 2T103 FOREMOST project is intended to ensure the major European chipmakers can reach this goal for 45 nm technology even ahead of the ITRS predictions. The consortium involves chipmakers, equipment and material suppliers, and research institute and universities.

Demonstrating design rules

FOREMOST is making use of the outputs from the EU Sixth Framework Programme NANOCMOS project, which carried out initial screening and demonstration of appropriate materials, device and interconnect architectures for 45 nm CMOS logic. The main target of the MEDEA+ project is to demonstrate the industrial manufacturability of a complex test vehicle representative of 45 nm design rules.

The FOREMOST DRAM work has two development goals:

1. New devices for peripheral transistors – in parallel and close interaction with the logic devices work – that will be required for future double data rate standards; and
2. Novel transistor structures for DRAM cell arrays, also related to the future of CMOS logic that requires development of 3D transistor structures for logic in the long term.

Within the timeframe of FOREMOST, the 45 nm CMOS 300 mm flash memory process targets are related to the full implementation and validation of high-k materials for the formation of the interpoly

dielectric in the memory cell structure, and on the integration and metallisation technology qualification of high aspect ratio and below 70 nm dimension contacts for high density memory. Achievements of a process ready for integration are expected by mid 2008.

Another important goal is to optimise and implement globally competitive European 300 mm industrial equipment in lithography, high-/low-k materials and characterisation techniques for the CMOS process, and enabling techniques to achieve 45 nm node specifications. FOREMOST will ensure chipmakers and equipment suppliers work towards a common goal of promoting the excellence of the European equipment industry.

Success in meeting these challenging project goals will allow development of the technical capabilities to prove 45 nm node CMOS manufacturability on 300 mm wafers by mid 2008. From experience in previous MEDEA+ projects, this leaves chipmakers enough time to bring the processes developed in the project to industrial exploitation, ahead of the 2010 timeframe predicted by ITRS for industrial production of the 45 nm technology node.

Key development work

Key development work will include use of optical lithography for module development and full CMOS process integration, based on 193 nm immersion tools. E-beam direct write lithography will be used in parallel for study and integration of the first modules. FOREMOST will also assess the potential of nanoimprint lithography by applying it to a specific metal level of the multilevel interconnection process.

Exploration of front-end process modules will include:

- Bulk silicon with nitrided silicon dioxide/polysilicon (metal) gates boosted by strained channels as the main option for CMOS logic and the peripheral devices of the DRAM architecture;
- Advanced CMOS logic device architectures such as multiple gate transistors and specific 3D devices foreseen for the DRAM cell, including close monitoring of silicon-on-insulator (SOI) architectures as possible options; and
- High-k metal gate dielectric structures based on new materials making it possible to reach equivalent oxide thicknesses (EOT) of less than 1.5 nm.

For the other key front-end process modules, FOREMOST is targeting scaled shallow trench isolation (STI), ultra-shallow junctions (USJ) and a new silicidation process that makes it possible to extend use of nickel silicide.

Back-end process work will target a double damascene multi-level metallisation (MLM) copper/low-k dielectric architecture based on low-k porous carbon-doped silicon oxide (SiOC) materials with k in the range 2.3 to 2.5. The project is addressing all the critical issues of the MLM process: pore sealing, damascene patterning, copper metallisation and its associated seed/barrier deposition, chemical mechanical polishing (CMP), reliability and signal propagation performance.

Integration choices for the CMOS logic will be assessed in two demonstrators:

1. A vehicle anticipating the complexity of products; and
2. A 45 nm demonstrator with typically 30 mm chip size, more than 100 million transistors, five to six million gate standard cells, a set of major digital and analogue input/output cells, clock frequencies in the 300 to 400 MHz range, more than 10 Mb SRAM embedded memory, embedded analogue low power phase-locked loops, analogue-to-digital converters and digital-to-analogue converters for a final product high-end 3G multimedia baseband processor.

The DRAM demonstration will be based on test structures allowing validation of the process and design options.

Rapid exploitation crucial

The semiconductor industry has long proved its capability to co-operate successfully in Europe-wide programmes. These have helped European chipmakers catch up in technology, and have led to an indispensable improvement in their performance.

Such co-operative programmes have to continue. If there was no MEDEA+ programme for the 45 nm node in Europe, it would be impossible to mobilise the power required to get the key actors in the European market, let alone in the global market, to work together towards the goal of obtaining a worldwide competitive European-developed technology.

An important objective of this MEDEA+ project is to insure a rapid transfer of results into industrial exploitation. Achievement of the strategic goals is essential to prepare electronic components and applications for 2010 and beyond. FOREMOST will have direct impact in high-complexity European components offering much increased performance and huge decreases in cost per function. And it will help European equipment and materials suppliers to be in a position to supply a global market.

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