Project result

Cluster for Application and Technology Research in Europe on NanoElectronics

CT208 | FDSOI transistor architecture qualifies for 14nm node CMOS technology [REACHING22]

With the semiconductor industry leader announcing its choice of transistor architecture – 22nm based on a fully-depleted (FD) 3D FinFET architecture built on bulk silicon – European industry urgently needed to assess the optimal transistor architecture for the 22nm node. The REACHING22 project was therefore launched to investigate fully-depleted devices at 22nm versus conventional planar transistors on bulk silicon, and the benefits they offer in low-power applications. This project is now coming to an end, having made significant progress towards meeting all its objectives, and with encouraging results: the 'winning' technology – called FDSOI – uses a planar FD transistor architecture built on a silicon-on-insulator (SOI) engineered substrate.

Although bulk CMOS technologies are reaching some intrinsic limits with gate lengths drawn below 25nm, the major issue is the need to scale geometries further while keeping acceptable dynamic and static power, on one hand, and device variability at ever lower operating voltages, on the other. The REACHING22 project researched the optimal transistor architecture and its integration for 22/20nm node core CMOS technology, and provided an electrical proof of concept.

Meeting all objectives

The overall objective of REACHING22 was to create appropriate conditions for the deployment of CMOS 22/20nm technologies in Europe. More specifically, this project's technical goal was to research the optimal architecture and integration path for the 22/20nm node core CMOS technology, aiming at an electrical proof of concept based on an initial test mask set. Although REACHING22 covered the first phase of the 22/20nm technology deployment, the test mask set goes well beyond the simple proof of concept, traditionally based on an elementary SRAM cell.

Preliminary assessment work on the FDSOI technology performance was conducted using previous-generation design rules (28nm) and a test mask. At the same time, the necessary process modules for the 22/20nm technology and an appropriate silicon-on-insulator (SOI) substrate for the 20nm node were being developed. Subsequently, an electrical benchmark comparison was conducted between the 20nm bulk and the 20nm FDSOI CMOS technology architectures, based on transistor performances and an initial evaluation mask set.

REACHING22's key objectives (which were fully met) were:

- To demonstrate the 28nm FDSOI transistor architecture. Here a 40% performance boost (at Vdd of 1V) was attained, compared to equivalent lithography planar bulk transistors. Performance gain was even higher at low operating voltages (100mV reduced Vmin on SRAM), leading to the decision to industrialise the 28nm FDSOI technology and to develop a fully-fledge design platform. Variability of FD NMOS on SOI was reduced by 40% compared to bulk NMOS;
- To design and develop a complex SoC (application processor) demonstrator of 69mm^2 in 28FDSOI to serve as a qualification vehicle for the technology. This resulted in an outstanding dynamic performance over an extended supply voltage range;
- To achieve 100% toolset compatibility with 28nm bulk by extending the lifetime of the current toolset in the manufacturing fab.

Leadership through innovation

These encouraging results led the consortium to seriously consider FDSOI architecture as the major technology option for the 20nm node, displacing the 20nm bulk concurrently under development, and which could not show a comparable power-performance advantage. (Considering 20nm FDSOI is also capable of delivering next-node performance, it was decided to name it 14FDSOI.)

FDSOI technology offers several advantages. It has, for example, the potential to address the cost-performance squeeze facing the 22/20nm node as long as substrate materials are available in adequate volume, quality and price. FDSOI also provides a low-risk option for semiconductor companies seeking to take advantage of the benefits of

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Key project dates:

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End: March 2014

Countries involved:

Belgium
France

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	
More Moore	✔
Technology node	22/20nm

fully-depleted transistor architecture, while leveraging existing design and manufacturing capabilities. Although SOI substrates increase the overall technology cost, it can be compensated by devising an integration scheme less demanding in operational steps, while still maintaining a multi-Vt offer. FD transistors can also solve scaling, leakages and variability issues associated with shrinking. Globally, the resulting CMOS technology is less complex and therefore enjoys a good manufacturability and yield. And system-on-chip (SoC) devices, such as high-performance, low-power wireless multimedia processors, exhibit different requirements from mono-functional processors plugged into the mains.

REACHING22 has maintained a vibrant ecosystem in 'More Moore' technology, essential for developing strategic state-of-the-art digital electronics, especially low-power electronics needed to conserve energy and extend battery life in handheld devices. It will also provide accurate analytical and technology computer-aided design models to help with the development, assessment and optimisation of the different technology options. Several test structures will also be implemented on silicon to assess FDSOI technology for SoC and ultra-low-power applications.

Comprehensive and coherent strategy

Through this strategic project, 22nm node technologies, process modules and the screening of possible options were actively investigated with the ultimate goal of introducing them into industrial production in 2014 or 2015, at the latest. This means the various actors can deal with the challenges of worldwide business requirements and consolidating their leadership in a key enabling technology, instrumental to the communications sector.

Now, with 22/20nm core CMOS technology at a crossroads and with the need for innovation to keep this technology moving forward, a continuous and sustained effort is of paramount importance to the health of this sector in Europe. That is why REACHING22 is part of a series of More Moore projects, which constitute a comprehensive and coherent strategy in the development of successive digital CMOS technology nodes. With REACHING22 completing all its milestones, the initial research phase on the 20/14nm node technology is being concluded. However, the design enablement phase – in the form of the CATRENE DYNAMIC-ULP project – is already in progress, with the objective of deploying a low-power design platform. Furthermore, the ENIAC PLACES2BE project provides a pilot line for 'productisation' and a path to the industrialisation of '2X-1Xnm' FDSOI technologies in Europe.

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