Project result

Cluster for Application and Technology Research in Europe on NanoElectronics

CT207 | D/TSV integration platform goes a long way in successfully meeting IC manufacturing challenges [COCOA]

As the semiconductor manufacturing world faces significant challenges integrating heterogeneous technologies, there is a call for the industry and R&D institutions to collaborate to ensure the industry meets its goals in a timely manner. That is why the COCOA project was keen to develop a complete and mature 3D integration technology platform covering the entire range of processes required – from vertical interconnects and robust bonding to innovative packaging approaches – to address a wide range of products.

For decades, Moore's law has predictably driven silicon scaling, and semiconductor manufacturing has been based largely on planar (2D) technology. However, increasing need for less power, smaller form-factor and higher performance continues to drive ICs towards 2.5D and 3D.

The main objective of this project was to achieve chip-level three-dimensional, through silicon via (TSV) integration, wafer-to-wafer and die-to-wafer bonding, and packaging of stacked circuits, in order to create a complete technological platform for high performance and cost-effective 3D system manufacturing. The stacking, interconnecting and packaging technologies of 'multiple chip-on-chip' will open new opportunities in Europe in terms of applications and performance.

An impressive first

COCOA specifically addresses:

- 3D interconnects shrink and related specific development-process steps to increase density and cover the existing gap between medium (104 cm^2) and high-density (106 cm^2) technologies;
- 3D performance (thermal, mechanical, electrical and the like) improvement;
- Creating product demonstrators: specific prototypes developed for multimedia and wireless applications as well as sensor-integration applications which open new manufacturing opportunity to European partners.

And COCOA's technical results are impressive:

- The first real 3D integration of a processor with a wide I/O memory interface (WIOMING) was realised in 2012, with excellent results;
- Some of the most challenging steps for sensor integration with a μhot plate were achieved;
- Bonding and debonding steps for thin wafers.

Achievement through collaboration

An excellent collaborative spirit was present right from the start (and some partners continue to work together even though the project has ended). Communications were efficient and effective. Well-attended face-to-face meetings and monthly conference calls facilitated informal discussions between partners, and proved to be excellent tools to exchange ideas and propose new experiments, driving innovation and creativity (COCOA generated 12 patent applications). In addition, 70-odd publications and (conference) presentations also helped with information dissemination and exchange.

There are several achievements worth mentioning. The WIOMING demonstrator was the first 3D integration of its kind. Furthermore, some milestones were reached ahead of schedule. CMOS-compatible integration of the gas-sensitive SnO_2 layer and the sensitive measurement of CO (10 - 90ppm) with a DC power consumption of only 23 mWatt is an impressive result: the state-of-the-art reports much higher power consumptions in the 100 mW to 1 W range.

Finally, despite the challenge of 3D integration bonding/debonding (especially for thin wafers),

CT207 | D/TSV integration platform goes a long way in successfully meeting IC manufacturing challenges [COCOA]

Partners:

ASM-B
Austrian Institute of Technology
Austriamicrosystems
CEA-LETI
Datacon
EVGroup
HFWN
IM2NP
Semitool
SPTS
ST-Ericsson
ST Tours
STMicroelectronics
TUW

Project leader:

Brigitte Descouts
STMicroelectronics

Key project dates:

Start: March 2010
End: June 2013

Countries involved:

Austria
Belgium
France
UK

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	
Health and aging society	
Safety and security	✓
Energy efficiency	✓
Digital lifestyle	
Design technology	
Sensors and actuators	✓
Process development	✓
Manufacturing science	✓
More than Moore	✓
More Moore	
Technology node	

COCOA was able to successfully demonstrate the direct bonding of thin wafer, using standard alignment equipment.

Reaping the benefits

COCOA delivered direct gains for project partners:

- Concepts successfully developed in COCOA for temporary and chip-to-wafer (C2W) bonding can also be used for future customer demonstration;
- A partner, who has become one of three main suppliers in the field of TCB equipment, expects a yearly revenue in TCB equipment of more than €10m following the launch of a new TCB bonder; another partner is expecting sales of its silicon photonic systems to reach $215m by 2017;
- COCOA provided a semiconductor supplier with a good opportunity to develop its very first 3D pilot line and demonstrate the benefits of moving to 3D. This means offering complete solutions for new applications requiring high performances, high density and/or highly heterogeneous systems;
- Thanks to the excellent reliability results that were demonstrated for TSV-Middle, this solution is being transferred to CMOS sensor pilot lines to address automotive applications with stringent reliability specifications and requirements;
- 3D/TSV applications are expected to show significant CAGR over the next years for specialised process equipment for which one partner has a suite of dedicated tools that will speed up the industrialisation of the 3D/TSV processes;
- COCOA development work and deliverables will help commercialise equipment at industrial sites once volume-production starts, though integration with upstream/downstream process steps, and mandatory cost-reduction needed to meet industrial requirements;
- And two partners' collaboration in temporary bonding resulted in the creation of a joint lab.

COCOA also delivered other market and industry gains. As a key enabling technology, three-dimensional chip systems integration has gained significant momentum. Over 50 companies have been involved in developing 3D interconnects, and surveys forecast that the market for 3D integration will increase at a compounded annual growth rate of 52%. Furthermore, the development of a 3D integration technology platform capable of sustaining product prototyping and industrialising multiple chip-stacking will contribute significantly to the preservation of European semiconductor industry activities and could even contribute to the re-localisation of employment from Asia to Europe. In addition, this innovative technology will create new opportunities by using the expertise of European companies in the fields of high added-value product design and manufacture.

Finally, the flexibility characterised by this approach will ultimately combine different technologies dedicated to highly-specialised, high-performance functions per layer by using front-end technologies available in Europe. This will make it possible to replace conventional system-in-package (SiP) solutions, usually integrated by Asian companies. The co-integration of multiple CMOS technologies will greatly extend production among 300 mm, 200 mm and even older European fabrication facilities as innovative 3D products will use dedicated technologies to achieve complex system integration.

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.