Project result

CATRENE
Cluster for Application and Technology Research in Europe on NanoElectronics

CT205 |

Key embedded NVM products give European suppliers a competitive and technological advantage [REFINED]

Despite the complexity in developing embedded non-volatile memory (NVM) products, and the dire economic situation, increasingly more competitors are trying to enter this arena. To counter this threat and maintain its competitiveness and technological superiority, Europe has not only been developing solutions based on Moore's law's technology-shrink path, but also studying low-cost approaches and innovative cell concepts. Now, thanks to European leadership in this field and the REFINED project (and previous related projects), the first embedded non-volatile flash memory products deploying 65/55 nm, as well as the introduction of the 45 nm technology nodes and some low-cost options have been released.

Non-volatile memory (NVM) technologies play a crucial role in developing reliable, high-performance microcontrollers used in various applications, including smart cards, and in the automotive and consumer electronics sectors. There is now a notable effort in Europe to integrate NVM into baseline CMOS technologies, creating programmable product platforms for a more generic system-on-chip (SoC), and thereby increasing European chip-makers' competitiveness in derivative technologies. Embedding flash memory in SoC devices facilitates the use of application-specific software in more generic SoCs, thereby combining volume production with product differentiation.

The main goals of REFINED were to:

- Integrate NVM options in deep sub-90 nm standard CMOS baseline technologies, without performance degradation of the baseline CMOS;
- Integrate flash with 55 nm CMOS logic on 300mm wafers;
- Bring innovative cell options, such as nano-crystals, or process options, like high-K dielectric, closer to industrialisation through close co-operation between research and industry partners;
- Develop new low-cost cell solutions aimed at overcoming current limitations, such as endurance, without increasing the overall process cost;
- And develop test structures and methodologies to characterise and verify analogue performance of embedded NVM technology platforms.

Meeting milestones

Work in REFINED was divided into three main areas:

- Technology development of 65/55 nm and 45 nm eNVM processes, and low-cost eNVM processes for existing technology nodes;
- Developing new modules and cell concepts: focusing on the introduction of innovative elements in the process, namely high-k dielectrics, silicon nano-crystals and disruptive technologies; and conducting a benchmark and state of the art investigation into the various options;
- IP development, testing and characterisation: dealing with the design and layout of the various test structures, macro-cells and demonstrators; and tackling the issue of reliability and testing at intrinsic cell level.

And REFINED met all its milestones:

- Preliminary work for the development of the 45 nm new floating gate memory is complete and 55 nm eFlash technology has passed the qualifications steps successfully and is ready for production;
- Three eFlash technologies (from 90 nm to 150 nm) are in the production phase and a roadmap has been defined for the 65 nm embedded memories;
- Development of the LF110 CMOS core process with two embedded memory options (SST and single poly NVM) is proceeding according to plan.

Partners:

ATMEL
CEA-LETI
Infineon Technologies
LFoundry Rousset
STMicroelectronics

Project leader:

Dominique Goubier
STMicroelectronics

Key project dates:

Start: January 2010
End: December 2012

Countries involved:

France
Germany
Italy

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	✔
Health and aging society	
Safety and security	✔
Energy efficiency	
Digital lifestyle	
Design technology	
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	✔
More Moore	
Technology node	

European co-operation and leadership

REFINED brought together major R&D actors – chipmakers and research organisations – to develop the 65/55 nm generation, as well as improve the current 90 nm generation through technology shrink. In addition, this project supported the broad IP portfolio of project partners by reducing the time required to validate and industrialise new NVM cell concepts and process options. For this, REFINED relied on close co-operation between its industrial partners and research centres, in which reuse of existing technology platforms for industrial validation of the new concepts and process options was central. The variety of solutions studied will enrich the European offering and capability to fulfil any possible market requirement. The final goal is to maintain and consolidate the leadership of European companies in offering the most advanced embedded NVM SoC solutions worldwide.

Cross-European co-operation was a prerequisite for a successful completion of this challenging project, especially since the knowledge and competences of the different partners are complementary and cannot be found within a single European country. Usefully, the partners had already worked together in MEDEA, MEDEA+ and EU Framework Programme projects, which focused on embedded NVM and analogue process options, from 180 nm down to 90 nm baseline CMOS, with preliminary research into 65 nm and 45 nm cell concepts and process options. This project was in fact built on this long European co-operation and the good results achieved notably in the MEDEA+ MaxCaps project and, in the more design-oriented ENIAC JU SMART project essentially based on phase-change memory.

European leadership in embedded NVM is well recognised. In recent years, consortium partners have released the very first embedded NVM products for 180 nm, 130 nm and 90 nm technology nodes. These were based on work done in previous international co-operative projects. The target and present forecast is that one of the partners, a key semiconductor supplier, should be able to be the first to announce the availability of a 55 nm embedded flash technology working with 300 mm wafers.

For products with a large memory-to-logic area ratio – such as subscriber identity module smartcard products for mobile phones – it is expected that 90 nm shrink technologies using 200 mm wafers will be very cost-competitive with respect to 65 nm technology. A REFINED partner is working on such an intermediate technology node, and expects to be the first in the industry able to offer such products.

And shrinking embedded, single, poly-electrical erasable programmable read-only memory (EEPROM) at 150/130 nm using 200 mm wafers is a very cost-competitive way forward for devices requiring a moderate NVM size, and which need optimally stored information granularity demanded for applications targeting code access (such as nomadic applications, smart cards and industrial control).

Now, despite the increasing shift of manufacturing operations towards low-cost areas, the increase of added-value in SoC products (made possible as a result of REFINED) will allow European companies to lower manufacturing costs. In addition, they will be able to be more focused on other innovative products, which represent reliable, high-margin opportunities.

And the collaboration seen in REFINED is set to flourish beyond this project. Consortium partners in Grenoble and Dresden continue to participate actively in the two nanoelectronics clusters established at these locations in March 2010, further strengthening their co-operation in advanced technologies and industrial processes.

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CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.