Project result

Cluster for Application and Technology Research in Europe on NanoElectronics

CT302 | Towards one European test solution [TOETS]

As semiconductor chip packages become more and more complex, the process of testing gains greater significance at all stages of manufacture and throughout the lifetime of the product. The CATRENE TOETS project was therefore established to investigate ways of unifying test procedures both within and outside the chip circuitry and is largely based on the concepts of built-in self-test (BIST) and built-out self-test (BOST). The project consortium assembled includes several of the leading European semiconductor manufacturers and integrators as well as research institutions supporting the industry.

A testing dilemma

The TOETS project was set up with the aim of creating a breakthrough in methods and procedures employed to test system-on-chip (SoC) and system-in-package (SiP) devices by treating the process of testing as an integral part of the whole value chain from design to application. To achieve this ambition it was essential to:

1. Supply test services to the final integrator and the end-user that would be valid throughout the lifetime of the product,
2. Develop chip design methodologies that provide enhanced matching of functional and test requirements, enabling a reduction in the cost of testing and achieving improved test efficiency through BIST and BOST solutions and the better use of test resources,
3. Acquire relevant information about the components at transistor level to adjust performance and improve product quality.

The major goals of TOETS, that needed to be achieved by the end of the project, were targeted at improvements in dependability in application areas such as automotive and healthcare where operational integrity is essential; reducing test costs or at least stabilising the cost of testing compared to the overall cost of integrated circuit (IC) development & production and shortening test development lead times (total time to market - TTM)

Lower costs, higher reliability

Another aspect of the project was to improve system integrity by embedding self-repair and self-calibration features within the chip technology. Methods were developed to diagnose system issues as well as provide solutions that would compensate for faults and restore system functionality in the event of component failure. In this respect, the consortium partners also worked on different heterogeneous systems (medical, automotive, etc.) but with the same objective of reducing system test costs and improving overall system reliability.

Devices used by consortium partners to demonstrate their solutions included:

- Low cost self-test and self-calibration sensors (micro-electro-mechanical (MEM), magnetic, capacitor, temperature, etc.) embedded in a system to ensure system integrity and the highest accuracy.
- An accurate self-calibration unit for level switchers used in the functional electrical stimulation (FES) context, to guarantee optimal communication between an implant and human tissue during the entire product life.

Developments achieved demonstrate the feasibility of system-level inbuilt calibration and self-repair. An overall improvement in product quality has been shown on several systems, including those involving sensor applications. Moreover, a reduction in the cost of testing has been achieved at system level as a result of the integration of the new embedded calibration techniques.

Reducing the cost of testing

Managing the cost of test (CoT) compared to the overall cost of chip manufacturing (CoGS, cost of goods sold) is the key to success in the very competitive semiconductor market. Consequently, the focus of the TOETS project was to develop testing

MANUFACTURING SCIENCE

Partners:

ATMEL
CEA-LETI
CEA-LIST
CNM-IMSE
D4T
e2v
INESC Porto
JTAG
KU Leuven
LIRMM
NXP Semiconductors
Ophtimalia
Q-Star
Salland
STMicroelectronics
ST-Ericsson
Supelec
Temento
TIMA
Tomorrow Options
University of Twente

Project leader:

Kees Veelenturf
NXP Semiconductors

Key project dates:

Start: March 2009
End: February 2012

Countries involved:

Austria
Belgium
France
Portugal
Spain
The Netherlands

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	✓
Health and aging society	✓
Safety and security	
Energy efficiency	✓
Digital lifestyle	
Design technology	✓
Sensors and actuators	
Process development	
Manufacturing science	✓
More than Moore	✓
More Moore	
Technology node	

methods that would contribute to cost reduction while at the same time increasing reliability.

The new device test architectures and alternative innovative test methods developed in the TOETS project provide new low-cost test solutions that allow the industrial partners to reduce their test cost, despite having only digital test equipment and by reducing test execution time per piece through higher parallelism of chip testing, even on high voltage ranges. Quantifiable and promising results have already been achieved by optimising the ratio of CoT/CoGS. Even so, there is evidently a demand for test equipment to cover the whole range of analogue and mixed signal (AMS) systems.

Currently, the only test programme generation tools available on the market are limited to purely digital test applications. None of the commercial (mostly US-based), tool vendors address the generation of analogue and mixed-signal test programmes. There are also no signs of test tool and electronic design automation (EDA) vendors indicating development plans for AMS test programme development tools. The concepts and prototypes for AMS test simulation based on defect simulation methodology, AMS/RF test programme synthesis and generation, developed in the TOETS project, will give the partners an advantage over the competition by reducing their test development time.

The computer test techniques toolbox based on statistical approaches and tools for BIST circuit evaluation will also give the partners an edge in test cost competition reducing test time and allowing low cost digital tester resources use.

Enhanced safety and reliability

Overall, it can be seen that the extent of the work performed within the TOETS project has covered a very broad range of component and application areas. Specialist applications, like those used in the aviation and automotive fields, will benefit from the enhanced safety and dependency resulting from the work done during the project. Medical uses of implanted FES devices will also directly benefit from TOETS project developments that considerably enhance reliability and precision. The development of BIST and BOST techniques, together with in-built automated repair, are advances that evidently greatly increase the lifespan of components and the equipment that they support.

By working together as part of the TOETS consortium, the various partners have shared knowledge that has enabled each of them to strengthen their individual role on the world stage and, at the same time, to enhance the position of the European semiconductor industry in the highly competitive world market.

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CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.