PROJECT RESULTS

CA112

Customisable heterogeneous high-performance design platform facilitates high-throughput fault-tolerant applications [HARP]

In developing a customisable, heterogeneous design-platform, HARP's unified hardware and software architecture does not only improve design productivity. Crucially, its data-flow programming models and reconfigurable memory hierarchy also ease and quicken the design of future high-throughput, fault-tolerant systems running performance-demanding, high-reliability applications, ranging from aeronautics to video.

High-performance computing (HPC) has evolved remarkably over the past 20 years. However, mobility trends are pushing the computational boundaries even further with demands to process video, speech, healthcare, vehicle and environmental data faster and more reliably. Indeed, mobility is not only highlighting the need for electronic equipment to be very reliable, but to also reduce inherent risks. This, in turn, calls for high-performance design platforms to develop and run high-throughput, fault-tolerant applications, in an ever-reduced power envelope.

HARP increases performance and design productivity

Addressing these important issues, HARP developed a heterogeneous architecture which can be optimised for a given customisation level. It does this by integrating, in the same system-on-chip (SoC), one or several clusters composed of a mix of general-purpose and specialised processors, together with hardware intellectual property blocks (IPs).These IPs were developed by semi-automatic design-flow using high-level synthesis tools, and a data-flow programming model based on data-flow graphic descriptions. In this way, HARP achieved the best of both worlds: software offering flexibility and easy post-production customisation; and hardware providing high performance and a smaller footprint (hence lower costs).

HARP produced a set of new design techniques based on standards (like OpenMP), which it then applied to demonstrators, validating such application areas as aeronautics, computer vision and multi-standard video codecs.

The project also analysed the issues of multi-processing, both by quantifying and circumventing them. For example, performance-loss due to shared program cache memory was minimised. The metrics obtained on demonstrators confirmed the soundness of the HARP approach. At the design level, for instance, parallelisation showed a time-reduction from months to weeks; and simulation was faster by a factor of 600. And at the application level, throughput went up by a factor of 40; energy efficiency by a factor of 58; and silicon area was reduced by 20-30%.

Allowing Europe to stay ahead of the competition

In general, HARP will contribute to Europe's potential to compete in worldwide markets and, thus drive employment. This means it will not only safeguard high-qualification jobs in the European microelectronics industry, but also generate new jobs at small and medium-size enterprises (SMEs) and create opportunities by sharing high-tech results. Design productivity will also benefit from HARP's unified hardware/software design flow, dataflow programming models and reconfigurable memory hierarchy, thus facilitating the design of high-throughput, fault-tolerant applications. This enables high-performance products to be designed faster, and at a favourable price and with lower energy consumption.

But there are more benefits in store. HARP's deliverables will allow European industry to extend its portfolio of innovations with, for example, new encoding algorithms which could be used in many-core SoC implementations, thus allowing Europe to secure its reputation in MPEG video technology. In addition, performance-estimation techniques for mapping video applications onto heterogeneous platforms, and hardware IPs that increase the average performance of video applications will help broaden Europe's knowledgebase and product portfolio. And another 'soft' deliverable – its hardware/software co-design methodology – could be extended to deal with the movement of massive amounts of video-related data across the computing fabric.

Aeronautics is another key HARP target, where the high-level of hardware redundancy, a key safety requirement, represents up to two-thirds of the electronics' cost in a commercial aircraft. Thanks

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Safety and security
- Energy efficiency
- Design technology

PARTNERS

STMicroelectronics

AIRBUS GROUP

SAPEC

CEA

Universitat Autònoma de Barcelona

University of Cantabria

COUNTRIES INVOLVED

France

Spain

PROJECT LEADER

Philippe Garcin
STMicroelectronics

KEY PROJECT DATES

January 2013 - June 2016

to HARP's fault-tolerant computer architecture based on advanced arrays of multiprocessors, costs will come down and European suppliers of aeronautic systems will have a competitive edge.

Imaging is yet another area to benefit from deploying HARP-developed technologies. Smart cameras, deployed in the internet of things (IoT), will use less energy, and reduce bandwidth requirements and minimise privacy risk by doing image analysis on-chip.

Consumers will also be winners. Video-related products will be lower in price and come with increased video quality (compared to the current H264-AVC standard). There are also plans to double the ratio of data compression (with a resolution of up to 7680 x 4320 pixels).

Finally, conserving energy. Computing power is strongly correlated to energy consumption, and mobile equipment has limited access to permanent power sources. Energy efficiency is therefore a main part of HARP's requirements, and elements, such as low-power multi-core processors, will be key enablers in sustainable and energy-efficient projects.

Promising markets for imaging, video and fault tolerance

The business in which HARP will play a role looks promising. With device-to-device communications (where HARP's deliverables could be deployed) becoming widespread, Gartner forecasts 20 billion devices connected by the end of 2020.

Thanks to HARP, companies could also increase their share of the video market and help European electronics firms maintain their leadership position in set-top boxes (STBs). It does this by ensuring they are among the first (and ahead of the competition) to provide multi-standard video-codecs within the new, high-performance, highly efficient SoC generation, offering UHD5 (a version of ultra-high definition television) support and a short time-to-market. Furthermore, future video applications will create new business. The worldwide revenue for STBs is expected to exceed US$ 4 billion annually from 2016 on. With an 8% market share, a leading European electronics concern and project partner predicts revenue of US$ 1 billion and a 5% growth per year in STB unit shipments. And thanks to HARP-developed technology, revenue, gross margins and market share will also grow.

Then there is the worldwide market for HDTV H264 video encoders, which stands at around US$180m, with an expected CAGR (compound annual growth rate) of 6-7% in the next five years. New algorithms that reduce the bandwidth, and new TV systems like UHDTV and 3DTV, will drive this CAGR growth. And the 65% market share for Intel-based, video-analysis systems is projected to decline and huge gains are expected in the digital signal processing (DSP) market in 2014-2016. In addition, the market for computer-vision technologies will grow from US$5.7 billion in 2014 to US$33.3 billion by 2019, representing a CAGR of 42%.

And finally, aeronautics. The world's passenger aircraft fleet (above 100 seats) will grow from 18,500 aircrafts to 37,500 by 2033. At the same time, some 10,500 aircraft from existing fleets will be replaced by more eco-efficient models. Importantly, HARP's fault-tolerant system could be marketed by aircraft suppliers as a unique selling point, based on its benefits.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org