PROJECT RESULTS

CA703

Lower development costs and faster time-to-market expected with Open ESL technologies [OpenES]

This project's objective was to provide the European industries with open electronic system-level design and verification methods and tools. These enhanced system-level design capabilities increase productivity, reduce system design costs and increase product quality, thereby improving competitiveness of European semiconductor and system-design companies.

Building on Europe's strengths in integrating advanced complex systems is important to its competitiveness. And as demand for more features and improved functionality is making systems design and development more complex, there is an increasing need for advanced methods and tools to improve productivity (faster time-to-market) and quality (less design errors and less re-designs) in system-level design and verification in order to allow European industries to remain competitive. Electronic design automation (EDA), which involves a diverse set of software algorithms and applications, aids the designing of complex, next-generation semiconductor and electronics products, which is where OpenES plays an important role.

ESL and open standards improve chances of success

True to its name, OpenES developed a solution based on open standards and on a methodology called electronic system-level design and verification (or ESL), which makes use of appropriate abstractions in order to increase comprehension about a system, and also increase its chances of a successful and cost-effective implementation.

In particular, this methodology:

- Fills in gaps in design-flows with new interoperable tools and/or improve existing tools/flows ensuring the semantic continuity of the design flow;
- Specifically focuses on integral support of both, functional and extra-functional requirements – from specification to verification – jointly, with the use cases defined at system level;
- Raises reuse capabilities from intellectual property (IP) to hardware/software (HW/SW) subsystems in order to eliminate integration effort by supporting reuse of pre-integrated and pre-verified subsystems;
- Enhances interoperability of models and tools by upgrading and extending existing relatively new open standards (SystemC TLM, SystemC-AMS, IP-XACT).

Key project activities included:

- Implementing the OpenES Modelling Kit;
- Defining IP-XACT extensions for extra-functional properties and provide interfacing solutions for models and tool flows;
- Defining common requirement traceability flow for functional and extra functional (timing, power and thermal) verification, starting at high abstraction-levels (UML);
- Implementing case studies and evaluating OpenES design-flow performances;
- Promoting the project globally and sharing relevant information.

Notably, OpenES achieved the following:

- All 29 technical deliverables have been released;
- Six milestones have been successfully reached;
- Benefits to OpenES technologies have been quantitatively measured in five case studies, showing up to 33% in manpower savings;
- Joint standardisation actions have been undertaken, resulting in a significant European impact by defining new standards;
- Several new tools or updates have been implemented and are now available for commercial use, expanding market opportunities for several project partners;

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Design technology

PARTNERS

CISC Semiconductor GmbH
Docea/Intel
ECSI
Magillem Design Services
STMicroelectronics
Thales Communication & Security
Thales Research & Technology
NXP Semiconductors N.V.
Synopsys
Vector Fabrics
CEA LIST
UGA-VERIMAG
Technische Universiteit Eindhoven (TUE)

COUNTRIES INVOLVED

- Austria
- France
- The Netherlands

PROJECT LEADER

Laurent Maillet-Contoz
STMicroelectronics

KEY PROJECT DATES

1 April 2013 - 31 August 2016

- A global dissemination effort has spread the project results in Europe and in the US, reaching American and Asian communities. This effort produced:
  - 21 scientific papers
  - 25 presentations at workshops and seminars
  - 15 exhibitions and demonstrations
  - Four new courses/training materials

Lower development costs and faster time-to-market

The common open and extensible solutions developed are providing a design framework and interfaces built on standards wherever possible. Extensions of standards have been initiated where necessary. Thanks to this openness and the use of standards, every project partner can achieve an advanced and complete system design-flow, enhancing it according to specific requirements from a given application domain. This offers significant improvements in system-design capabilities and a good cooperation between integrated circuit/intellectual property (IC/IP) provider and system integrator. The broad relevance and functional capability of this common approach are demonstrated through case studies from various key domains of European industry: wireless/software defined radio; multimedia/set-top-box; automotive/traffic and security; and industrial/power control. Final results of the case studies have proven the relevance of the approach deployed, and confirm the benefits of the technologies developed in the project.

OpenES will also maintain state-of-the-art technology at universities and research institutes, ensuring high education standards. It will also impact European industry in two ways. Firstly, it will enhance the system-level design to reduce development costs by improving the co-operation between system houses and semiconductor companies; and by establishing an ecosystem based on open standards to create high-level models and associated tools, thus avoiding expensive development of in-house, proprietary approaches and tools.

And secondly, OpenES will optimise products to increase competiveness by innovating product architectures and increasing efficiency in product design, with less redesigns, reduced system-development cost and faster time-to-market. Furthermore, it will increase Europe's heterogeneous and embedded systems in a more optimised and systematic manner. Together, it will maintain Europe's leading position in product innovation and design in major applications.

Increasing role of ESL will drive the EDA market

The EDA market grew 9% in 2010 and 14% in 2011, reaching US$4.19 billion worldwide in license and maintenance revenue last year (excluding services and IP). The sector employed more than 26,000 people at the start of 2012. A steady 10% growth rate is predicted for the next five years, sustained by a continuous shift of design methodology to the ESL level. And the increasing role of ESL in overall IC design flow is indeed expected to foster the market for new dedicated EDA tools.

Notably, according to market intelligence, 2014 marked the first year of really solid growth for ESL tools in the EDA market. ESL technologies started experiencing their long-awaited user adoption in earnest. For the first time, ESL growth was higher than that of either the downstream computer-aided engineering market or the EDA market as a whole.

Finally, there is also good news on the IP and subsystems market fronts, where development costs of a single system-on-chip (SoC) is over US$85m and this cost is rising rapidly. Encouragingly, the industry has responded to these rising costs through the concept of IP blocks: functional components that act as building blocks which can be integrated into a SoC. The SoC market is expected to grow from $85.9 billion in 2011 to $117.8 billion in 2016, at a CAGR of 6.47% from 2011 to 2016.

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CATRENE (E! 4140), the EUREKA Cluster for Application and Technology Research in Europe on NanoElectronics, will bring about technological leadership for a competitive European information and communications technology industry.

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