PROJECT RESULTS

CAT601

A coherent Chip-Package-Board/System Co-design environment reduces costs and improves time to market, design reliability and performance [SiPoB-3D]

What compact system-integration needed to reduce costs and mitigate the risk of failure was an effective design environment with the facility to design over all three domains chip, package, and board/system. This allows extensive pre-fabrication testing and changes before compact electronic systems are finally released for manufacturing. That is exactly what the Co-design for System-in-Package-on-Board (SiPoB-3D) project delivered.

For reasons of performance, size and cost, technologies like More Moore (MM), More than Moore (MtM), three-dimensional high-density 3D IC, system-in-package (SiP), as well as passive integration are combined. Compact system-integration, as this process is called, also involves a variety of different materials. However, because of inherent complexities, this process is expensive and risk of failure high. It also raises challenges with the interface between packaged chip and board (PCB). Ideally, what is needed is a user-friendly, coherent Chip-Package-Board/System Co-design in which designs can undergo extensive pre-fabrication testing and changes – but without the associated costs – before they are finally released for manufacturing.

Coherent and effective cross-domain design environment

SiPoB-3D largely aimed at addressing seven key challenges which were considered major issues:

1. Need for a coherent design environment: chip, package, and board/system.
2. Need for improved data exchange and design interfaces
3. Alignment of different tool landscape for Chip-Package-Board/System Co-design
4. Handling a variety of technologies (at Chip-Package-Board/System Co-design level);
5. Avoiding expensive hardware prototypes;
6. Dealing with thermal management across domains;
7. Supporting proper material selection, especially in respect to mm-wave parameters and Coefficient of Thermal Expansion (CTEs).

To handle these and other issues, a well-balanced project consortium was appointed, bringing together the experience and expertise of semiconductor suppliers, major suppliers with strong board capabilities and applications which could be applied to better understand the requirements and related problems and solutions in connecting the three domains. In addition, project research and support were provided by several European academic institutions.

Excellent project results have been achieved. SiPoB-3D delivered the prerequisites for such a design environment, which supports development within a single company as well as jointly between companies. The environment also reflects a coherent consideration of chip, package, and board/system, critical for future semiconductor product-development. There are obvious future benefits. New innovative multi-chip SiP and 3D products, new applications, and larger application windows are expected from such a coherent design environment and new methodologies. In addition, new products from tool suppliers are expected and board suppliers can significantly improve their data management, as well as, benefit for technology improvements (like higher line/space density or chip embedding).

Crucially, the project itself generated several success stories. It investigated the design environment and applied it to different types of systems containing both complex logic and analogue devices. Furthermore, the project's device manufacturers developed and improved the methodology and implemented its design capabilities into their internal tool environment for right-first-time design. Now these companies can develop and optimise complete SiP devices (together with their customers) faster, better, and more economically.

There were other notable project activities and deliverables, such as assembly design kits for many relevant package technologies, including lead-frame packages and complex laminate ones. This is an essential base to optimise designs over all three domains of chip, package, and board/system. In addition, one of the project's semiconductor suppliers deployed an optimised SiP and the 3D design-flow suite within its entire design team, working with technology nodes in non-volatile memory or CMOS. This reduced the cycle time for complex 3D/SiP system-on-chip (SoC) designs by around 20%, and minimised the risk of re-spins by integrating low power and board-level checks for SiP/3D designs. In addition, this design environment is being used for very advanced nodes below 28nm. A flip-chip checker, which enables both substrate

PROJECT CONTRIBUTES TO

Automotive and transport

Digital technology

More than Moore

More Moore

PARTNERS

Infineon Technologies AG
Continental Automotive GmbH
Computer Simulation Technology GmbH
Hitex Tools Development GmbH
Schoeller Electronics Systems GmbH
Symeo GmbH
STMicroelectronics SA
STMicroelectronics (Grenoble 2) SAS
Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e. V. (FhG)
with its institutes EAS/IIS and IZM ASSID
FAU Erlangen-Nuremberg
CEA-LETI
Université de Savoie IMEP- LAHC, Chambéry, Le Bourget du Lac

COUNTRIES INVOLVED

Germany
France

PROJECT LEADER

Klaus Pressel
Infineon Technologies AG

KEY PROJECT DATES

01 March 2016 - 31 May 2019

and silicon designers to quickly validate the bump matrix and assembly rules, is fully integrated in the company's co-design framework environment, from front end to back end manufacturing.

Furthermore, simulation and modelling of electrical and thermal performance of integrated antennas were implemented in a mm-wave SiP toolbox. Special focus was on determining material parameters and their characterisation by innovative methods up to 100 GHz. Significantly, these results pave the way for the design of mm-wave products of much larger complexity, and for improving systems in terms of resolution, production cost and size.

Finally, project results are already being applied to design 5G and mm-wave applications (like 77 GHz radar or advanced logic in microcontrollers). The project will also open new market segments for mm-wave radar systems, like collision avoidance and smart agriculture as well as expanding suppliers' modelling and simulation portfolios, from electro-magnetic and thermal performance, to thermo-mechanical.

Significant collaboration and information sharing

Key to the success of SiPoB-3D was, on the one hand, the involvement of project experts on the chip, package and board/system level; and on the other hand, the verification in hardware. Information sharing was also excellent. The project consortium distributed some 80 reports and provided more than 30 presentations, including one at Cadence Forum 2019 where it received an award for the best presentation.

Impacting design environment, science and education

SiPoB-3D design environment ("backbone") has been introduced by semiconductor partners for already 80% of their complex devices. More than 60 design engineers of the involved chip suppliers are already actively using the backbone design environment for their Chip-Package and Board (PCB)/System co-layout tasks.

SiPoB-3D also impacted science and education: several Bachelor of Science, Master of Science, doctoral and post-doctoral students participated actively in the project as part of their education and related projects.

A promising SiP market

One focus of SiPoB-3D was on SiP applications, which increasingly affect the electronics market. Due to miniaturisation, SiP has become an enabler for heterogeneous integration, and the SiP market is growing, with 3D-SiP solutions appearing in products and components in various market sectors such as automotive electronics (3D image sensor chips), energy generation and energy distribution (Smart Grid), industrial electronics, where SiP growth of over 20% is predicted and in such sectors as solid-state lighting, medical and aeronautics.

All of this is reflected in market-statistics publications; Yole's 2019 report predicts a CAGR of about 11% during 2018-2023 for the total assembly market for RF-SiP components in mobile phones. In their market report from May 2019, Zion Market Research forecasts a CAGR for SiP of around 8.1% during 2019-2025. Growth is also supported by statistics from Allied Market Research, which expect the global SiP packaging-technology market to reach US$30 billion by 2022, growing at a CAGR of 9.0% during 2016–2022.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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