PROJECT RESULTS

CT210 New FDSOI design platforms can handle complexities of next-generation mobile devices [DYNAMIC ULP]

Technical advancements in mobile communications are in turn making mobile devices a lot more complex in design. In response to these demands, the DYNAMIC-ULP project developed two new design platforms for European manufactures. These are based on CMOS, commonly used in today's computer microchips, and FDSOI, a new competitive technology simplifying the manufacturing process.

By 2025, some 50 billion everyday appliances could be communicating wirelessly with other devices through the internet of things (IoT). Combine this with the mobile society's appetite for increasing amounts of multimedia content and additional functionality, and the result is a demand for even faster mobile networks based on LTE-advanced – the enhanced long-term evolution (LTE) mobile-communications standard – with transfer rates of more than 100 Mbit/s, and access to multimedia contents with no latency to the user. Crucially, this is making next-generation devices more complex, and a rapid increase in gate density will not address this complexity on its own.

Delivering two key FDSOI-based design platforms

What is really needed is an efficient design platform that will handle product requirements covering a wide dynamic range, from 1.1v (to enable processors to run at 3.25 GHz) down to 0.4v (for long multimedia playback). Among the key chip technologies deployed today FDSOI (fully depleted silicon on insulator) is the most advanced planar technology, and is able to significantly boost the performance or save a huge amount of power. DYNAMIC-ULP developed advanced process modules and contributed to two successive generations of FDSOI design platforms based on the 28nm and 14nm technologies for European manufacturers.

The project produced several key results and deliverables. At process and device levels, 14nm FDSOI technology was developed leveraging on the so-called body bias effects for a full FBB approach (high body bias). Looking to the future, studies and measurements conducted on SSGOI (strained Si/SiGe on insulator) showed that this process can ensure the scalability of the planar FDSOI device architecture for the 10nm node.

It fully confirmed SSGOI device-performance benefits. Compared to the 28nm FDSOI technology, the 14nm FDSOI device developed provides 0.55x area scaling, and delivers a 30% speed boost at the same power, or a 55% power reduction at the same speed. In addition, dual patterning was also introduced in the 14nm. The number of metal layers at 14nm node in UTBB FDSOI will be 11ML.

Furthermore, Dynamic-ULP provided the first FDSOI design platforms in 28nm and 14nm, including FDSOI design kits with spice models. A comprehensive test-chip strategy valid for both the 28nm and 14nm was used during the project in order to assess the performance of the technology and qualify the design platform. All IPs (intellectual properties) in 28nm FDSOI were validated, and the 28nm FDSOI has been qualified for volume production (Maturity 30) since end-2013.

FDSOI-based methodologies included methods for SRAM (static random-access semiconductor memory) development and design of specific logic (intellectual property firmware) blocks: variability analysis of SRAM bit-cells and SRAM 32kb circuits; feasibility studies to integrate forward and back biasing and DVFS (dynamic voltage and frequency scaling, a power-management technique); and development of a new test chip to connect the relevant IP blocks into a front-end receiver chain designed for LTE application.

New or improved commercial tools are ready for deployment. A new CAD (computer-aided design) tool for SRAM and standard cell verification (based on Monte-Carlo simulation) was developed, which shows an 8x speed improvement on standard tools for the industry. The efficiency of high performance/low power solutions was proven in most conditions and adapted in the case of low energy gains. Several techniques were developed that reduce the memory power of the design automatically. New cells were proposed for high energy efficiency and variability management also progressed, thanks to new mathematical methodologies. Furthermore, this project demonstrated improvements in 23 metrics.

PROJECT CONTRIBUTES TO

Communication

Energy efficiency

Digital lifestyle

Design technology

Process development

More than Moore

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COUNTRIES INVOLVED

France

Sweden

Turkey

PROJECT LEADER

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KEY PROJECT DATES

January 1, 2012 - December 31, 2014

DYNAMIC-ULP was a close collaboration of five partners from France, Sweden and Turkey. The project's R&D activities included 36 conferences and publications, invitations to give four lectures, and four Master's and PhD theses on subjects relevant to this project.

Stimulating the whole value chain

There are also commercial gains. After 15 years of constant growth, the mobile wireless market is now mainly fuelled by the replacement of outdated devices with smartphones and tablets, and also the emergence of new devices such as the "wearables". This has created a new segment with double-digit growth, and this project supports the European effort to gain a leading position in electronic industry by enabling design and production of FDSOI CMOS technologies in Europe.

The strategic nature of the semiconductor industry has been recognised around the world, and this recognition has led to the continuous emergence of new geographic regions as future semiconductors hubs, acting as a powerful engine for economic growth and high quality jobs. In addition, the research intensity in semiconductor is proportionally higher than in any other industry and provides an adequate incentive to reinforce the presence of upstream industries, such as semiconductor equipment manufacturers and material providers. The association of R&D activities with volume production and strong manufacturing facilities also has a profound impact in developing local ecosystems.

Vital for manufacturing

The IC industry has been one of the fastest growing industries over the past 30 years, primarily because it has been able to offer a continuously decreasing cost per function to the electronics industry. This rise in economic value is the main reason, explaining the success and proliferation of integrated circuits in our daily lives. For manufacturing, improving and developing tools and methods to effectively manage this highly complex mix of technologies, processes and products – something DYNAMIC-ULP is contributing to achieve – is playing a critical role in ensuring the future viability of the manufacturing facilities of our industry in Europe.

Europe cannot keep innovating without a powerful manufacturing base. This makes it necessary to maintain advanced prototyping activities in Europe, since it is the basis of future production runs and it may well help relocate production activities into Europe. DYNAMIC-ULP's design platforms in FDSOI 28nm and 14nm technologies will help achieve this, by joining with system architects, chip designers, CAD vendors and manufacturers.

Looks promising

Among the metrics where this project scored high marks, twelve of them concerned power reduction, indicating the importance it placed on ultra-low power techniques. Not surprisingly, it offers attractive solutions for the mobile industry, but also for the consumer market, IoT, green applications and more. Notably, good results recently obtained by Sony from an ST 28nm FDSOI test-chip implementation of a global navigation satellite system show that the penetration of FDSOI technology associated with efficient design methods is underway.

Finally, there are clear benefits from having the ability to remain competitive and at the leading edge of technology for job creation and retention in the European Union. The project involves multiple European countries and enables further employment opportunities in the future due to the new innovations being advanced in the project, especially enabling advanced manufacturing to continue, and a more fertile market for SOI wafers.

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CATRENE (E! 4140), the EUREKA Cluster for Application and Technology Research in Europe on NanoElectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.