PROJECT RESULTS

CA109

Hybrid architecture, many-core TSAR processor and algorithm parallelisation feature in new high performance computer [SHARP]

The SHARP project played a significant role in investigating and prototyping a new high-performance computer (HPC) hybrid architecture – an extension of the existing BullX HPC system – and in the design of the many-core TSAR processor in 2.5D silicon technology. On the application front, SHARP addressed algorithm parallelisation and the porting of existing sequential code to the hybrid HPC architecture.

Performance in scientific computing (measured in 'flops' or floating-point operations per second) has increased significantly: from teraflops in 1997, to petaflops by 2008. Industry and market demands are now driving exascale systems (a thousand-fold increase over the first petascale computer), when the number of processing cores is also expected to increase dramatically. Many countries world-wide are investing in high-performance computers (HPCs) to maintain their key positions on the world stage in diverse industrial sectors.

Indeed, Europe needed to invest in HPCs to model and simulate the scientific advancements required to develop its future products and services. It was quite clear that economies that make such an investment are those that will, over time, gain the greatest competitive advantage and reap the largest economic benefits. Hence the current scramble to invest in large-scale leading-edge HPC systems world-wide.

This was the technical and technology backdrop and business case that triggered the SHARP project in 2012, and guided it to its completion in 2015.

Focus on performance, power consumption and scalability

SHARP is based on the premise that the future of high performance computing lies in heterogeneous and massively parallel computer systems that can support efficiently the large spectrum of (potential) applications. This highlights the ever-increasing need for performance, with efficient power consumption a close second. This project set out to create a generic and flexible HPC architecture based on key considerations – performance, power consumption and scalability, together with reliability, flexibility, heterogeneity and security. Developments in SHARP addressed not only hardware and software (especially programmability) aspects, but also application implementation for the purpose of validation and demonstration.

In order to compare against the state-of-the-art, SHARP used the Top500 classification of supercomputing. This is based on a recent high performance conjugate gradient (HPCG) criterion (to balance floating point processing, communication bandwidth and latency with a focus on messaging, memory and parallelisation) which provides a new classification of existing HPC solutions.

Major technical achievements and deliverables include:

- Design and prototyping of a generic HPC architecture integrating a variety of computing technologies (many-core CPU, GPGPU, FPGA);
- Complete design of the TSAR processor in a 2.5D silicon technology (tape-out);
- Software development (OS, specific application layers, etc.) in relation to various computing technologies, and to support security features;
- Optimal implementation of a large range of applications on heterogeneous computing technologies: Examples include video processing (multi-core CPU+FPGA); traffic light recognition (many-core CPUs); medical image processing (CPU+GPU); and system prototyping (CPU+FPGA).

Collaborating closely with Europe

The five-member European project consortium had wide expertise and experience, ranging from hardware development for open servers and HPC solutions, heterogeneous systems design and analysis, to parallelisation and embedded solutions dealing with telecom, multimedia and security applications.

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Health and aging society
- Safety and security
- Energy efficiency
- Digital lifestyle
- Design technology
- Technology node

PARTNERS

Bull
Thales Communications
CEA/Leti France
UPMC/Lip6
FZI

COUNTRIES INVOLVED

France
Germany

PROJECT LEADER

Huy-Nam Nguyen
Bull

KEY PROJECT DATES

September 2012 - August 2015

Co-operation between SHARP partners was excellent due to the fact that the core consortium had worked together previously on past projects. There were also links with other European and national projects which, for instance, provided funding for the silicon design of the TSAR processor. SHARP also worked with other external partners, like CEA/Dam and UPEC, in such specialist areas as eG and medical image processing, as well as in implementing the proprietary QPI protocol on the field-programmable gate array (FPGA). The latter it did in close collaboration with Intel and Altera.

On the promotion, information sharing and innovation front, three patents were filed; four PhD theses, based on the work done in SHARP, were successfully defended; and 18 technical papers were published.

The drive to invest in HPC

SHARP's deliverables provide European industry with the means of securing and maintaining its competitive edge. Thanks to its HPC solution, this project will enhance computing performance in a very large range of applications – from complex system modelling and simulation, to real-time data mining and image processing. This allows industry to maintain its key position on the world stage in sectors as diverse as automotive, pharmaceuticals and financials, as well as, biological and renewable-energy. It also provides industry with the drive to invest, or continue to invest, in HPC: it is the only way to model and simulate the scientific advancements needed to develop future products and services.

The rewards also look promising. The global high-performance computing market is projected to reach US$ 36.62 billion by 2020, at a CAGR of 5.45%. The emergence of big data has also increased the demand for HPC clusters to handle a data-intensive workload and support high-performance simulation and data analysis. Equally encouraging, the cloud-related HPC market is estimated to grow from US$ 4.37 billion in 2015 to US$ 10.83 billion by 2020, at a compound annual growth rate (CAGR) of 19.9% from 2015 to 2020.

Going the extra mile

Unusually, many of SHARP's developments go far beyond their initial objectives, such as finding and applying solutions, like HPC components, to real-life industrial problems, and exploiting prototypes, tools, methodologies and educational materials in industry. This illustrates and reflects the drive of the project partners and the efficiency and effectiveness of the project results.

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