PROJECT RESULTS

CT305 | Towards reducing 450 mm wafer production costs by 30% and improving European competiveness [SOI450]

The SOI450 project aims to develop silicon-on-insulator (SOI) substrates for the transition to 450 mm silicon wafers. It is expected to stimulate European infrastructure to take a lead in this and related work, in order to ensure Europe will be fully-prepared to participate and contribute actively to the wafer-size transition in this innovative and technology-driven market segment. Although this project was halted temporarily in mid-2014, it did have several key achievements.

Silicon-on-insulator (SOI) is an innovative way in chip fabrication for replacing bulk silicon wafers with multilayer ones. These SOI substrates are strategically used in the transition to 450 mm wafers in order to meet cost per transistor requirements, and be able to continue to exploit Moore's famous law. By increasing the wafer surface by a factor of 2.25, the 450 mm wafer is expected to reduce production costs by 30%, compared to the 300 mm.

Notably, the transition to 450 mm manufacturing means huge efforts and total alignment with future standards. However, this can only occur (at the right time) when many important and significant factors come together, including a:

- Compelling manufacturing return on investment;
- Strong supplier readiness;
- Critical mass of device makers who need to make the transition.

Gearing up for a successful 450 mm transition

The SOI450 project started in November 2011. The goal was to bring 450 mm SOI and related technologies to an appropriate maturity for a 450 mm transition in the middle of the decade, with the first dies on 450 mm expected around 2015.

To reach this goal, a consortium of eight partners from four European countries provided access to expertise and other resources in market leading silicon research, design and fabrication, as well as, to a supply of equipment and process solutions linked to SOI substrates production.

The project was divided into three work packages:

1. Management, roadmap alignment, targets and assessment;
2. Specific-equipment design & development;
3. SOI processing implementation

Following the alignment and technical maturity assessment phase, some important project work was done and key tools delivered. In particular, cleaning solutions were developed on an EVG bonding tool using megasonic cleaning (a type of acoustic ultrasonic cleaning). In addition, the Adixen Pod Analyzer (APA) was deployed in the 300 mm fully-depleted silicon-on-insulator (FDSOI) substrate line. This will improve yield and optimise FOUP (a specialised plastic enclosure to hold silicon wafers securely and safely) in cleaning costs. The final design of the SOI bonded system was also achieved and validated. Crucially, the bonding quality of the cleaning module and the IR inspection reached the specification targets for 450 mm.

Furthermore, the research & development inspection platform is also available. The software and data management system was updated to be compatible with wafer size, resolution needs and higher volume of exchanged data. Finally, the complete SOI process was demonstrated and validated, all process steps tested and the bonding tool installed and produced excellent cleaning / bonding results;

In terms of prototypes. Altatech developed the table-top 450mm metrology system, Altasight, which can interface with major players in material and process developments. And Adixen's study and assembly of its APA450 prototype, and its installation at G450C (Albany, USA), gives the company a forefront position in the area of molecular contamination, and an big advantage with international customers.

Unfortunately, the SOI450 consortium decided to halt the project temporarily in June 2014, at the behest of the project co-ordinator (Soitec). This was due to doubts expressed by integrated device manufacturers about the then-market for the 450 mm, which was followed by subsequent delays in the project roadmap, and inherent economic and technical consequences.

PROJECT CONTRIBUTES TO

- Energy efficiency
- Design technology
- Process development
- Manufacturing science
- More than Moore
- More Moore

Technology node / 22 nm

PARTNERS

INTEL PLS`
EVG
ALTATECH
ADIXEN
ASM
LETI
IMEC
SOITEC

COUNTRIES INVOLVED

- Austria
- Belgium
- Ireland
- France

PROJECT LEADER

François Brunier
SOITEC

KEY PROJECT DATES

November 2011 - December 2014 (temporary)

Perfect poised to restart

On a positive note, the consortium will be ideally positioned when SOI450 is finally restarted, and for several reasons. The project has achieved a level of maturity in SOI 450 mm technologies and equipment. Furthermore, what has been technically demonstrated with the 450 mm is mostly 'retrofitable' in the 300 mm; and project partnerships increase sharply the value of these developments. Crucially, Soitec remains connected, through the SOI450 project, to the G450C (the global consortium focused on building the 450 mm wafer and equipment development environment).

Technical and technological triumph

Now, there are very good reasons why this project should be completed. On the technical and technological side, SOI450 will ensure the fabrication of SOI substrates at the right moment for time to market. SOI will deliver a powerful tool to balance power efficiency and performance: it provides increased transistor switching speed of more than 30%, power reductions of 50% or a trade-off in lower/performance and superior isolation for circuit and design. It also enables compact integration of intellectual property (IP) blocks. Furthermore, SOI will play a key role in the 'more Moore' race as it responds to most of the scaling challenges. These ultimate nodes are the ones targeted by 450 mm transition.

Good for European business and competiveness

SOI450 also involves the development of equipment and materials for the next generation of semiconductor devices, and new business opportunities. These products define a huge, self- sustaining market by themselves. In these global markets, the European equipment and materials industry has achieved a world-leading position and acts as a powerful European engine for economic growth in its own right.

The introduction of the 450 mm wafer diameter will be a new opportunity for the European equipments and materials industry to improve its competitiveness and gain market share.

A case in point is Soitec. This European manufacturer produces 80% of SOI substrates and is the global leader in this field. As SOI substrates are one key path to nanoscale CMOS – identified by end users for digital applications, system-on-chip devices and memories – large volume applications are forecasted, deploying possibly the 450 mm. It is therefore essential to capture this market with the transition to 450 mm.

The project also aims to stimulate the European infrastructure concerned with 450 mm development on SOI materials and related advanced technologies, such as bonding, cleaning and thermal treatment. The objective is to increase European leadership and competitiveness within this highly innovative and technology-driven market segment. This target requires a joint effort for the development of innovative substrates and equipment.

Now, SOI 450, together with other European 450 mm projects, will have a significant impact on further R&D activities. It will provide access for the companies involved and European research institutes to the necessary 450 mm SOI technology. Without European and national funding, worldwide co-operation and the access to 450 mm would be very limited because a large part of the development work would then be performed in Asia or the USA.

Finally, such projects are an important way for the European equipment and materials industry to participate in next-generation wafer technology, and in the worldwide market for 450 mm equipment and materials. It is envisaged that, because of their huge size, there will only be a small number of 450 mm high volume fabrication facilities built around the world. It is therefore very important that Europe ensures that at least one such facility is built and operated in the region.

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