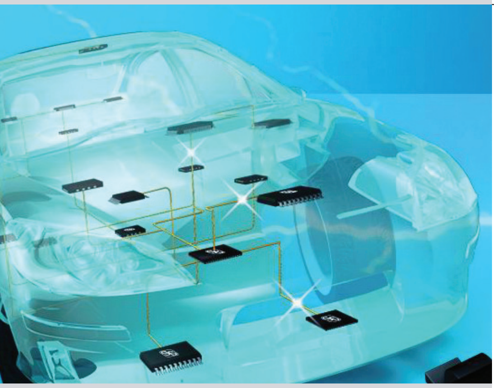
PROJECT RESULT

Technology platform for process options

2T204: End of life investigations for automotive systems (ELIAS)



Guaranteed-lifetime semiconductors for the automotive market

Carmakers around the world seek ever more advanced vehicle electronics to assist in areas such as safety, fuel consumption and reduced carbon-dioxide emissions. For the chipmakers, these pressures translate into demands for greater integration, more advanced functions and, as reliability issues come to the fore, systems that are guaranteed to be robust. Yet providing this guarantee, until now, has been a hit-or-miss affair involving deliberate over-design of circuits. Now the MEDEA+ ELIAS project has come up with a method of predicting, with great accuracy, the lifetime of electronic components.

Most innovations for the automotive market, especially in traffic safety or reducing carbon-dioxide emissions, require ever increasing functionality from automotive electronics systems. Higher power densities, stronger electric fields and higher temperatures all increase the difficulty of testing and verifying for quality and reliability.

Conventional accelerated-test methods such as increased temperature and voltage are already close to their physical limits. The MEDEA+ 2T204 ELIAS project undertook to develop a new, simulation-based ageing model approach to quality and reliability testing for advanced automotive semiconductor components.

Range of ageing models

The ELIAS approach, which was largely inspired by standards in the automotive electronics sector such as AEC-Q100 or the forthcoming ISO 26262 (Functional safety) focused on failure modes, their characterisation and their modelling.

ELIAS's main targets were to:

- Develop highly accelerated reliability tests for specific failure mechanisms;
- Develop accurate lifetime-simulation models;
- Derive prognoses for different operating conditions; and
- Integrate the completed simulation tools and methods into a functional and effective design flow.

The MEDEA+ project involved a strong consortium of major semiconductor manufacturers, a thermal engineering specialist, an electronic automation instrumentation supplier, key European research organisations and a car manufacturer.

By the end of ELIAS, partners had developed a range of quantitative ageing models and test methods for the major stress mechanisms at silicon and package level. In addition, they had validated these models using diverse semiconductor technologies, taking into account differing ageing effects which arise with higher temperatures and voltages.

A key achievement was the development of an ageing simulator for advanced 'smart-power' chip designs; this has already been integrated into the project partners' design environments and introduced to the computer-aided design marketplace.

International guidelines

ELIAS has also produced a set of international guidelines for fast wafer-level reliability monitoring. This is an innovative method used to test the reliability of semiconductor components and prototypes within a very short time frame. Based on continuous production monitoring, the technique provides improved costefficiency while upholding quality requirements.

Specific semiconductor designs can now be assessed much more easily as to their suitability for more extreme conditions such as higher temperatures. Any design changes necessary can be determined without the need for additional experimental stress tests and analysis of failed devices.

In addition, ELIAS results make it possible to predict the reliability of components over very long periods of operation – for example 17 years. Previously, testing for such predictions was either impossible or too expensive to be a realistic option for commercial automotive markets.

Higher reliability by design

With the results of ELIAS, the project partners' ability to extend simulation of the ageing process significantly will bring real advantages in the marketplace. Mentor and Cadence, for example, are now both offering an ageing-model interface for components with arbitrary numbers of pins and content. With this kind of simulation ability, chip designers can carry out quantitative investigations into the cost impact of reliability issues during the design phase, instead of being forced to design-in an unknown margin.

The partners are now integrating this reliability-optimised design flow into their future automotive-design kits. In addition, the successful standardisation of the reliability-simulation interface, together with the accompanying ageing models and other design tools, will lead to a faster adoption of these techniques by a broader range of design houses thanks to dissemination via the partners' software interfaces.

Improved knowledge of temperatures and temperature distribution under real application conditions will enable semiconductor designers to develop smaller chip areas without jeopardising reliability. The ability to produce newer and more highly integrated packages will also enable the partners to bid for applications with higher temperature and power requirements, generating business from new market sectors.

Application possibilities in the automotive marketplace include fuel-injection control, gearbox control, headlamp positioning and alternator regulation, to name but a few. New materials will also be important for applications in the industrial field – such as electrical supply network management – where long lifetimes are a critical requirement.

Improved safety applications

The results of ELIAS will support the design of highly reliable application-specific integrated circuits and underpin faster introduction of new smart power technologies. Such technologies are directly applicable to the microelectronics industry and their customers in the automotive, industrial and consumer markets.

In the automotive market, such capabilities will result, over time, in more reliable vehicles with higher levels of safety-oriented equipment. They can also be applied to forthcoming markets in green power generation and the smart grid.

ELIAS won the Jean-Pierre-Noblanc Award for Excellence in 2009 at the Nanoelectronics Forum in the Netherlands. The prize reflected the importance and quality of the project outcome, the more than 45 publications issued and numerous contributions to workshops and conferences.

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COUNTRIES INVOLVED:

Austria
Belgium
France
Germany
Italy