



Technology platform  
for process options

## 2T205: Deep sub-micron smart-power technologies (SPOT-2)



# Europe retaining its position in smart-power technologies

Combining sophisticated control logic with the management of high voltages and currents, smart-power technologies are at the leading edge of semiconductor design worldwide. The challenge for the designers is to meet the increasing demand for both voltage handling and greater integration – without sacrificing quality and product lifetimes. The MEDEA+ project SPOT-2 aimed to develop innovative and cost-effective power handling technologies for such applications, while maintaining and stabilising the position of European semiconductor manufacturers in increasingly competitive global markets.

The integration of complex system-on-chip (SoC) semiconductor designs requires the ability to interface easily with applications in the external world, often to control functions such as displays, actuators and motors. When these functions require the management of high voltages and/or currents in combination with sophisticated digital control logic, semiconductor designers can face huge challenges in the form of heat tolerance and reliability.

The MEDEA+ 2T205 SPOT-2 project aimed to develop innovative and cost-effective power handling technologies for SoC designs, enabling systems houses to offer increased speed and reliability despite the temperature risks involved in handling higher voltages. The project focused on what are called ‘smart-power’ applications, which are typically found in the automotive sector and in other applications where the operating conditions are, for electronic systems, relatively harsh – i.e. subject to higher vibrations and temperatures.

### Complete supply chain

The project partners in SPOT-2 are key players in the semiconductor and automotive markets. The consortium was deliberately constructed to involve the complete supply chain in the automotive sector, from chipmakers to wafer manufacturers, automotive tier-1 suppliers and the carmakers themselves.

Initial explorations found two distinct preferred approaches to the challenge of progressing smart-power technologies which combine CMOS digital logic functions with higher voltage DMOS drivers. The first approach, favoured by one set of partners, was to base the work on bulk-silicon substrates. The second preferred the alternative silicon-on-insulator (SOI) substrate materials.

Both approaches were combined at the commencement of the project, and a comparison of specific benefits for typical applications was added to the work programme. In each case, the challenges involved increasing voltage handling while shrinking geometries to 180 and 130 nm levels from current production technologies at 0.35  $\mu\text{m}$ .

### Common specifications

The key tasks for SPOT-2 were to ensure reliability at high voltages and handling of higher currents and high junction temperatures while managing this greater geometric density. Support from systems partners within the relevant automotive supply sector provided common specifications for future production technologies.

By the end of the project, the semiconductor partners had developed and some also qualified 0.15/0.18  $\mu\text{m}$ , 120 V technologies on SOI or bulk material for automotive applications.

Significant advances were also made on the checking of 0.15 µm CMOS-device functioning with the introduction of SOI, and on the other manufacturing steps required for high voltage devices. The first commercial products are under development, and the industrial partners believe the new processes are going to be a key development for their business. For example Infineon has developed a smart-power product using its own ninth edition smart-power technology (SPT9) capability, which covers all relevant components of this technology: large areas with logic circuitry, static random-access memory (SRAM), non-volatile memory (NVM) arrays and large power devices. During the development phase, several unexpected technology weaknesses were found and addressed. Other partners made similar advances.

## High performance/high power

The results achieved in SPOT-2 will support a wide range of smart-power applications using differing semiconductor technologies. All the technologies have benefited from a shrinking of geometries, enabling the provision of more functions on the same silicon area. These new smart-power technologies will underpin the introduction of new products that combine high-performance computation and high-power management capabilities.

Applications that are already in preparation for development include:

- Power and voice over Ethernet (IEEE 802.3af);
- Automotive safety, power train and comfort;
- Sensors with intelligence and memory; and
- Conversion systems for solar power and wind energy generation.

All of these applications will benefit from reduced power consumption, higher integration and a reduced cost per function.

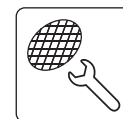
An important area of innovation made possible by SPOT-2 will be reduced vehicle fuel consumption, thanks to improved engine-control electronics and sensors. The advances made in this automotive-sector application, by providing the technological foundation for further tightening of EU carbon-dioxide emissions targets, will contribute significantly to the environmental goals of the European Union.

In addition to improving the project partners' own products, SPOT-2 results will extend the market for smart-power devices among the broad range of leading design-houses around the world, thanks to dissemination by the foundry service of some partners.

## Pushing smart-power limits

The results of this MEDEA+ project are pushing European smart-power technologies beyond previously existing limits. While the project was under way, additional competitors entered the smart-power market, showing the importance of this application sector to semiconductor foundries.

A final analysis of the outcomes of SPOT-2 places the project partners at the leading edge of this market worldwide. This result will position European semiconductor manufacturers and automotive industries within the global vanguard and help to safeguard employment in the sector. The project demonstrates that a 'More than Moore' strategy – a focus on system integration rather than transistor density – can be successfully implemented in Europe.



Technology platform  
for process options

### 2T301: EUV advanced generation lithography in Europe (EAGLE)

#### PARTNERS:

Atmel France  
Audi  
Robert Bosch  
Bruco  
Continental Automotive  
Infineon  
LAAS-CNRS  
NXP  
ON Semiconductor  
SOITEC  
TELEFUNKEN Semiconductors  
TU-Vienna  
X-FAB Semiconductor Foundries

#### PROJECT LEADER:

Volker Dudek  
TELEFUNKEN Semiconductors

#### KEY PROJECT DATES:

Start: April 2007  
End: September 2010

#### COUNTRIES INVOLVED:

Austria  
Belgium  
France  
Germany  
The Netherlands



**CATRENE Office**  
9 Avenue René Coty  
F-75014 Paris  
France  
Tel.: +33 1 40 64 45 60  
Fax: +33 1 45 48 46 81  
Email: [catrene@catrene.org](mailto:catrene@catrene.org)  
<http://www.medeaplus.org>



MEDEA+ Σ!2365 is the industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.