26-27-28 May 2008 IMEC, Belgium

MEDEA+ DAC: Nano-Electronics Towards System Integration: The EDA Challenge

Focus

Application-oriented design methods for SoC have become a very important success factor for European Micro- Electronic companies and will be looked at in its full range. Exhaustive research and development in this area has been supported by MEDEA+ and local governments. Latest results and exciting highlights from MEDEA+ projects will form the subjects of this conference.

Contents:

All MEDEA+ projects related to electronic system design, to design automation and to manufacturing topics related to design are invited to contribute to the conference. Each project organizes a full session made of one tutorial presentation (45 min.) and 2 technical presentations (20 min. each) or contribute to a global session with a tutorial or a technical presentation. MEDEA+ project leaders are invited and will be contributing to this conference.

Organisation

Local Organisation: IMEC, Belgium

Steering Committee

- J. Borel, J.B - R&D, F
- B. Candaele, Thales Group, F
- M. Coppola, STMicroelectronics, F
- T. Tassignon, IMEC, B
- A. Jerraya, CEA-LETI, F
- W. John, Fraunhofer Institut IZM,D
- P. Koch, MEDEA+, F
- A. Reutter, Bosch, D
- W. Rosenstiel, Uni. Tuebingen & FZI, D
- R. Seepold, Uni. Carlos III de Madrid, E
- K. Veelenturf, NXP Semiconductors, NL
- D. Vellou, CEA/Léti/DCIS, F

Venue

IMEC vzw
Kapeldreef 75
B-3001 Heverlee
Belgium

Please register at:
http://www.imec.be/MEDEA_DAC

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Preliminary Agenda

Day 1: 26 May 2008

Keynote1: Henk Heijnen Thomson, EDA Lighthouse
Keynote2: Biotechnology and Microsystemstechnology forming BioMST: Chances and Potentials, Dr. Harald P. Mathis; Fraunhofer-Institute for Applied Information Technology

Session 2: Panel: Linking Design flow to Foundry, Fablite vs Fabless
(contents TBD)
Social event: Dinner

Day 2: 27 May 2008

Keynote 3: Keynote on Technology, Luc Van den Hove, IMEC
Session3: Analog and Mixed signal design challenges (Organizer: Annette Reutter, Bosch)

-Innovative design methods and tools for future AMS systems: Serge Scotti, STM
-Progress state of System-AMS standardisation in OSCI: Martin Barnasconi, NXP
-How to support the Design Refinement of Embedded Analog/Mixed-Signal Systems: Christoph Grimm, Vienna University of Technology
-Towards a Top-Down Design Flow for AMS Circuits and Systems - State-of-the-Art and Challenges: Peter Jores, Robert Bosch

Session4: Design for Yield/analysis/reliability (Organizer: Philippe Garcin, STMicroelectronics)

-DFM optimization flow for standard cells libraries: Fabio Melchiori, STMicroelectronics, Italy
-Analog/RF Parametrical yield: solutions and limitations: Firas Mohamed, InfiniScale, France
-Methods for yield analysis and optimization based on local process variations and mismatch effects: Ulrich Seidl, MunEDA, Germany

Session5: Simulation based hardware/software power management exploration for SMP MPSoC architectures" (Organizer: Marcello Coppola, STMicroelectronics)

-Tutorial: Frédéric Petrot from Tima and Anne-Marie Fouilliart from Thales
-NoC design challenges and solutions for MPSoC architectures: Fabien Clermidy/Pascal Vivet.
-CARVISION: AN FPGA DEMONSTRATOR FOR AUTOMOTIVE IMAGE PROCESSING - PEDESTRIAN DETECTION IN ACTION: Stefano Amadori (from ST) and Suresh.PAJANIRADJA (from CEA)

DAY 3: 28 May 2008

Session6: Computing and Hardware dependant Software design and verification (Organizer: Bernard Candaele, Thales)

-Modeling, Analysis and Verification of Hardware-Dependent Software: Oliver Bringman - FZI
-Cache-coherent, shared memory, multi-core architecture: Alain Greiner - LIP6, Nam Nguyen - BULL
-Integration and verification of system IP through component based HDS framework in SoC platform: Anne-Marie Fouilliart and Dominique Ragot THALES Communications

Session7: Electromagnetic Reliability (EMR) (Organizer: Ch. Hedayat - FhG IZM ASE)

-Electromagnetic Realibility of Systems: Werner John (FhG IZM ASE)
-Power Integrity Challenge of PCB Design: R. Bruening (ZUKEN Germany)
-Identification and Simulation of Critical Interconnect Paths with Respect to Transient Noise on PCB-Level: M. Taki (FhG IZM ASE)
-Verification strategy of mixed-signal integrated circuits regarding high power pulsed stress: H. Morgenstern (FhG IZM ASE) - W. Simbuerger (Infineon Technologies AG) - G. Groos - Universität der Bundeswehr - Germany

IMEC vzw
Kapeldreef 75
B-3001 Heverlee
Belgium
Please register at http://www.imec.be/MEDEA_DAC

For more information please contact:
Ahmed Jerraya, Head of design programs, ahmed.jerraya@cea.fr
Tom Tassignon, Project Officer, Tom.Tassignon@imec.be

CEA-LETI
Phone +33 438 780 128
Fax +33 438 785 182
ahmed.jerraya@cea.fr

IMEC
Phone +32 16 28 12 54
Fax +32 16 28 15 15
Tom.Tassignon@imec.be