



# CT207 | Chip-on-chip technology to open new applications [COCOA]

## PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	
Digital lifestyle	
Design technology	✓
Sensors and actuators	
Process development	
Manufacturing science	✓
More than Moore	✓
More Moore	
Technology node	

## PROCESS DEVELOPMENT

### Partners:

ASM-B  
Austrian Institute of Technology  
Austriamicrosystems  
CEA-LETI  
Datacon  
EVGroup  
HFWN  
IM2NP  
Semitool  
SPTS  
ST-Ericsson  
ST Tours  
STMicroelectronics  
TUW

### Project leader:

Brigitte Descouts,  
STMicroelectronics

### Key project dates:

Start: July 2010  
End: June 2013

### Countries involved:

Austria  
Belgium  
France  
UK

As a key enabling technology, three-dimensional (3D) chip systems integration has gained significant momentum. Over 50 companies have been involved in developing 3D interconnects and surveys forecast that the market for 3D integration will increase at a compounded annual growth rate of 52%. The CATRENE COCOA project is focusing on the development of complete 3D circuit demonstrators with a high level of performance to meet challenging specifications. The results should enable the European electronics industry to move into a new technology era offering great global opportunities to expand the use of 3D silicon-based technologies in highly-integrated complex systems at a reasonable cost.

Three-dimensional integration is an emerging technology that will enable the realisation of highly-integrated and complex systems by vertically stacking and connecting various materials, technologies and functional components. 3D integrated circuits benefit from the tremendous advantages of this new technology, including multi-functionality, high performance, reduced power consumption, small form factor, increased yield, improved reliability, flexible CMOS co-integration, reduced overall costs and shorter time to market.

The CATRENE CT207 COCOA project therefore set out to define a robust 3D integration technology platform to meet the market needs of multimedia for wireless and sensor integration products. The objective is to achieve chip-level 3D through-silicon via (TSV) integration and wafer-to-wafer and die-to-wafer bonding as well as the packaging of stacked circuits to create a complete technological platform for high-performance and cost-effective 3D system manufacture.

Stacking, interconnection and packaging technologies for multiple chip-on-chip systems developed in COCOA will open new opportunities in applications and performance.

### Mature platform targeted

COCOA is expected to develop a completely mature 3D integration technology platform covering the entire range of processes required from vertical

interconnects – TSV, micro bumps, etc. – and robust bonding for innovative packaging approaches to address a wide range of products.

Compared with existing collaborative projects dealing with 3D integration, COCOA addresses two elements specifically:

1. Shrinkage of 3D interconnects and the associated development process steps for increasing density and to cover the existing gap between medium [ $10^4\text{cm}^{-2}$ ] and high density [ $10^6\text{cm}^{-2}$ ] technologies; and
2. 3D performance improvement – thermal, mechanical, electrical, etc.

The resulting technology platform will have a substantial impact on a wide range of applications. It will be demonstrated by the realisation of product demonstrators. Specific prototypes will be developed for multimedia and wireless applications as well as for sensor integration applications. This will open tremendous new manufacturing opportunities for European partners.

### Complete 3D systems

The development of elementary process bricks and integration flow driven by product requirements will be validated through the realisation of complete 3D system application-based demonstrators defined in close collaboration with or by end-users.



Three main demonstrators are targeted within the time frame of COCOA:

1. The first will validate the design and process flows at mid-project. It will also form the basis for the development of the second demonstrator, by stacking two CMOS layers with different technologies to pave the way towards the first real wireless 3D product;
2. The second will involve integrating a high-performance third-generation chipset including digital and energy-management functionalities. One layer will be realised on the basis of advanced technology for digital processing and the other will be integrated using a more mature technology for energy-management and analogue functions. Such an application needs high-performance 3D interconnects to ensure fast signal transmission across the 3D circuit; and
3. The third will extend the application domain of developed technologies to stack and package a CMOS circuit with sensor components to show the potential of 3D technologies to integrate heterogeneous systems. A gas sensor based on nanocrystalline tin dioxide ( $\text{SnO}_2$ ) will be stacked on a CMOS circuit. This approach will be compared with current TSV and redistribution layer (RDL) technologies.

### Innovative processes

Successful integration of these demonstrators requires the development of innovative processes plus associated characterisations and modelling. In particular, the CATRENE project will address the development of technological solutions to achieve a 3D industrialisation stage. This will involve enhancing the maturity of elementary process steps in technological stacks to meet application specifications and developing innovative solutions that will improve perfor-

mance, including increased density, reduced delay times and lower power consumption as well as decreased manufacturing cost.

The following new solutions will enable the demonstrators to meet the required specifications:

- TSV connection to the rear-side RDL for front-side sensor integration;
- TSV filling strategy dependent on target density and aspect ratio;
- Co-integration of thick RDL copper metallisation and TSV copper filling;
- Multiple RDL layers to functionalise rear-side wafers;
- Bonding solutions for 3D chip stacking with medium density TSV;
- Innovative packaging approaches compatible with 3D circuits; and
- Integration of thermal vias to ensure thermal dissipation and spreading.

### Building on strength

COCOA supports European efforts to master flexible 3D integration technologies that would capitalise on the strength of European industry in the sectors of mobile and multimedia design, microelectromechanical systems (MEMS) and sensor integration, following the 'More Than Moore' development trend in order to develop a wide range of complex systems-on-chip (SoC) devices.

The development of a 3D integration technology platform able to sustain product prototyping and initiate the industrialisation of multiple chip stacking will contribute significantly to the preservation of European semiconductor industry activities and could even contribute to the re-localisation of employment from Asia to Europe.

In fact, 3D integration is an innovative technology that will create new opportunities by using the expertise of European companies in the fields of high added-value product design and manufacture. The flexibility encouraged by this approach will ultimately allow the mixing of different technologies dedicated to highly-specialised, high-performance functions per layer, such as fast or low power digital, analogue, passive integration, power, MEMS and sensors, by using the front-end technologies available in Europe. This will make it possible to replace conventional system-in-package (SiP) solutions usually integrated by Asian companies.

The co-integration of multiple CMOS technologies will greatly extend production among 300 mm, 200 mm and even older European fabrication facilities as innovative 3D products will use dedicated technologies to achieve complex system integration.



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**CATRENE** focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

